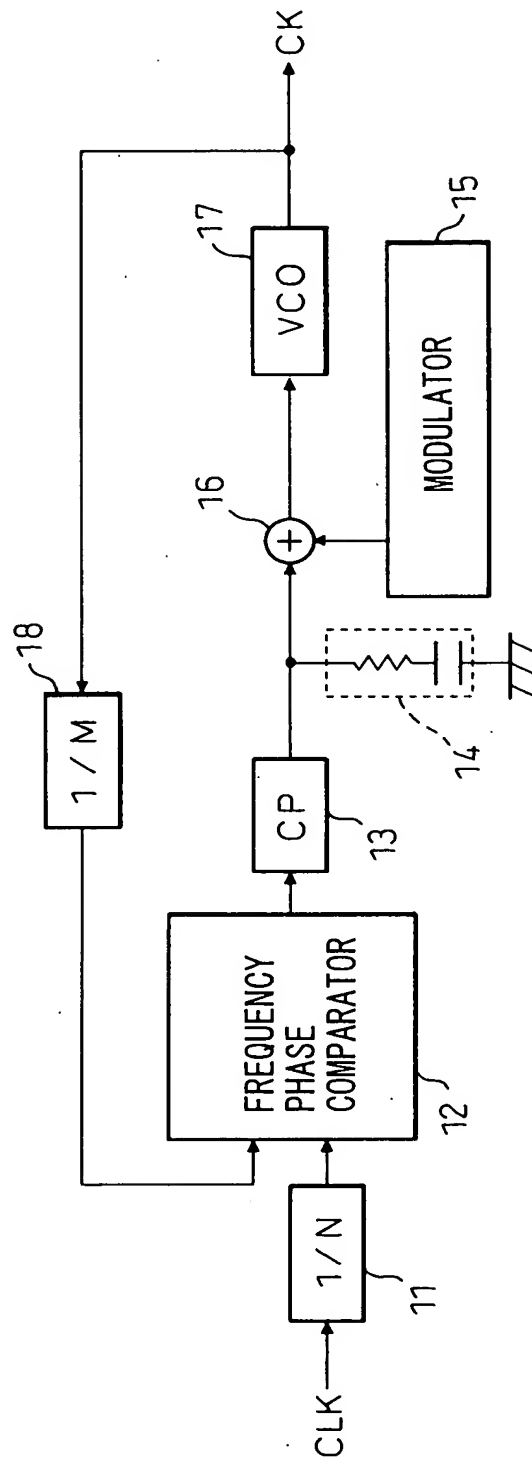


FIG. 1



Title: SPREAD SPECTRUM CLOCK
GENERATION CIRCUIT, JITTER GENERATION
CIRCUIT AND SEMICONDUCTOR DEVICE
Inventor: MIYATA, et al.
Appl. No.: Unknown
Docket No.: 100021-00138

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FIG.2

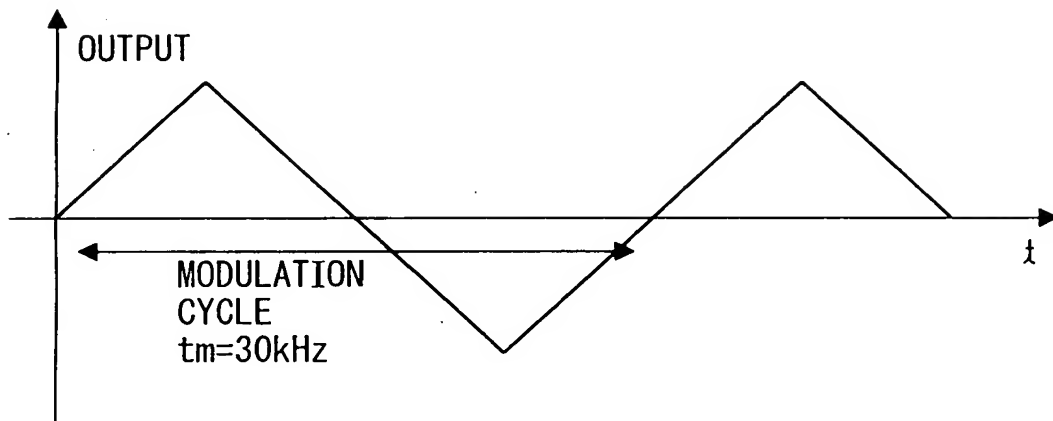


FIG.3

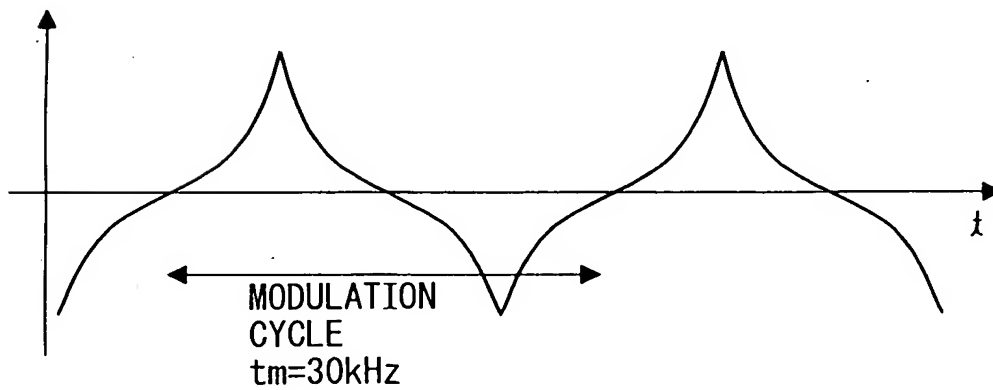


FIG. 4

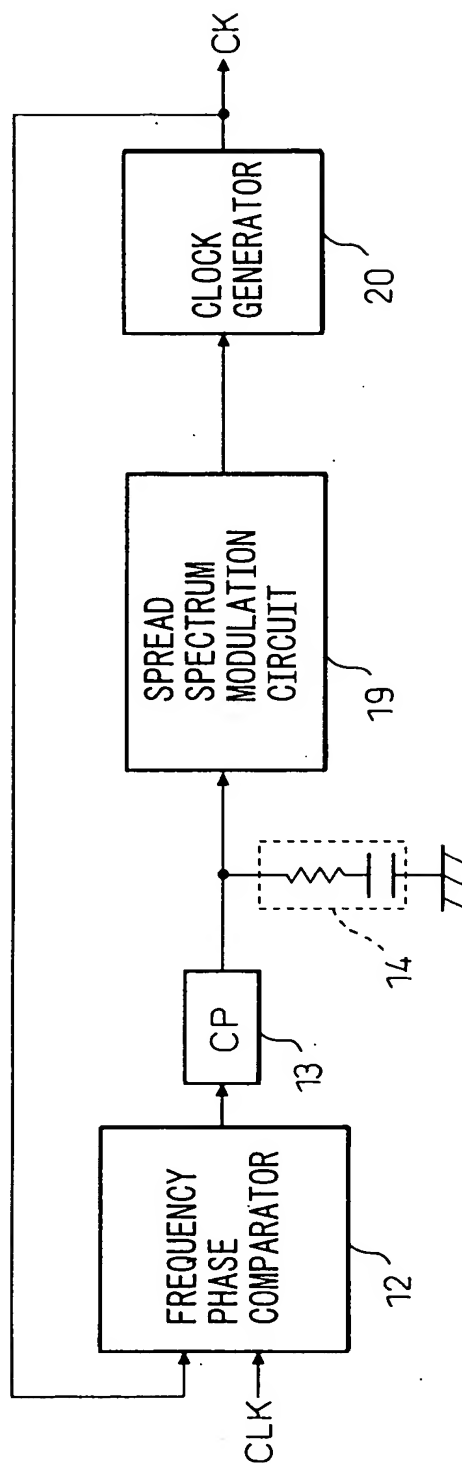


FIG. 5A

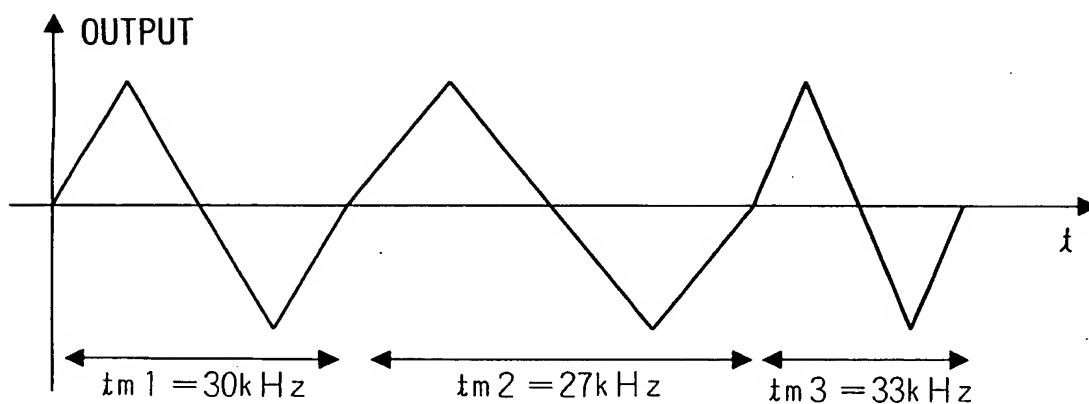
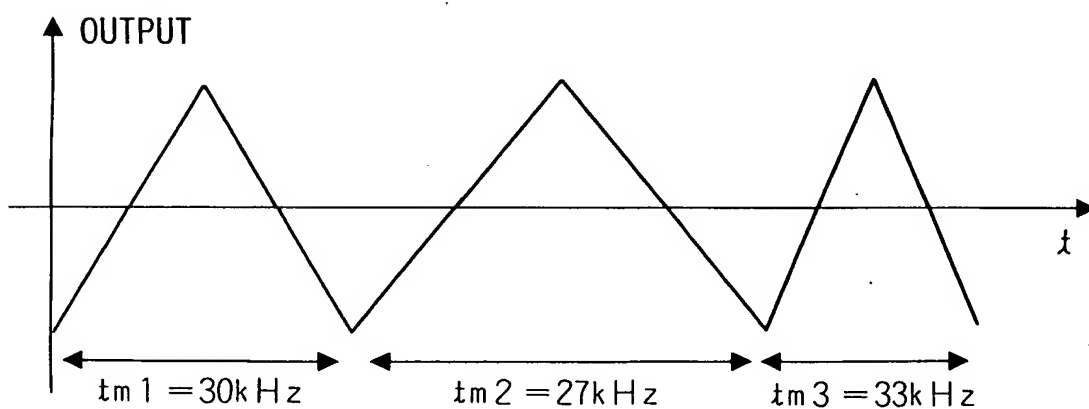


FIG. 5B



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FIG. 6B

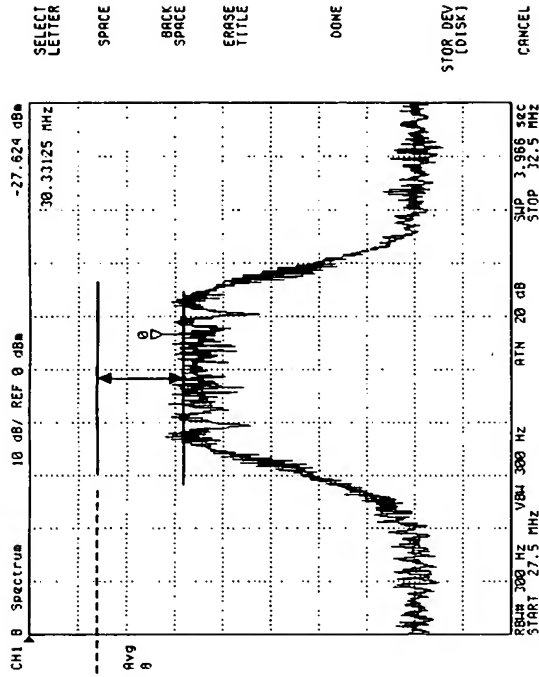
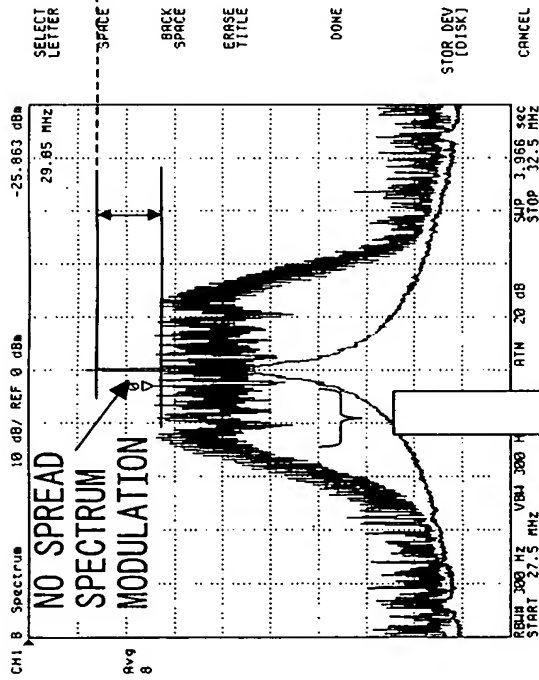


FIG. 6A



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FIG. 7A

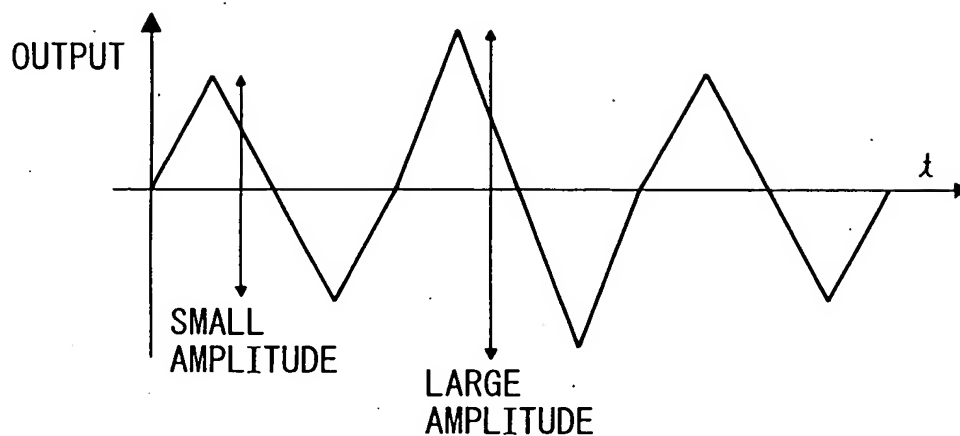


FIG. 7B

SPECTRUM WHEN A
SMALL AMPLITUDE
IS APPLIED

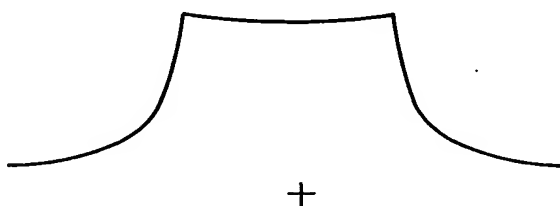


FIG. 7C

SPECTRUM WHEN A
LARGE AMPLITUDE
IS APPLIED

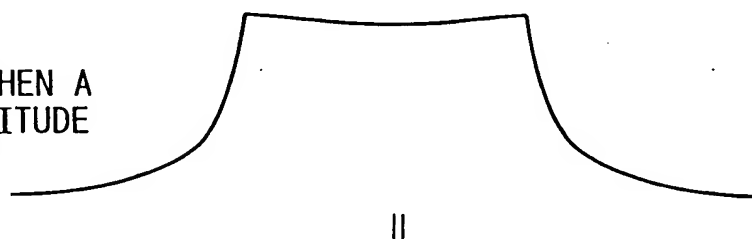


FIG. 7D

SYNTHESIZED
SPECTRUM



FIG.8

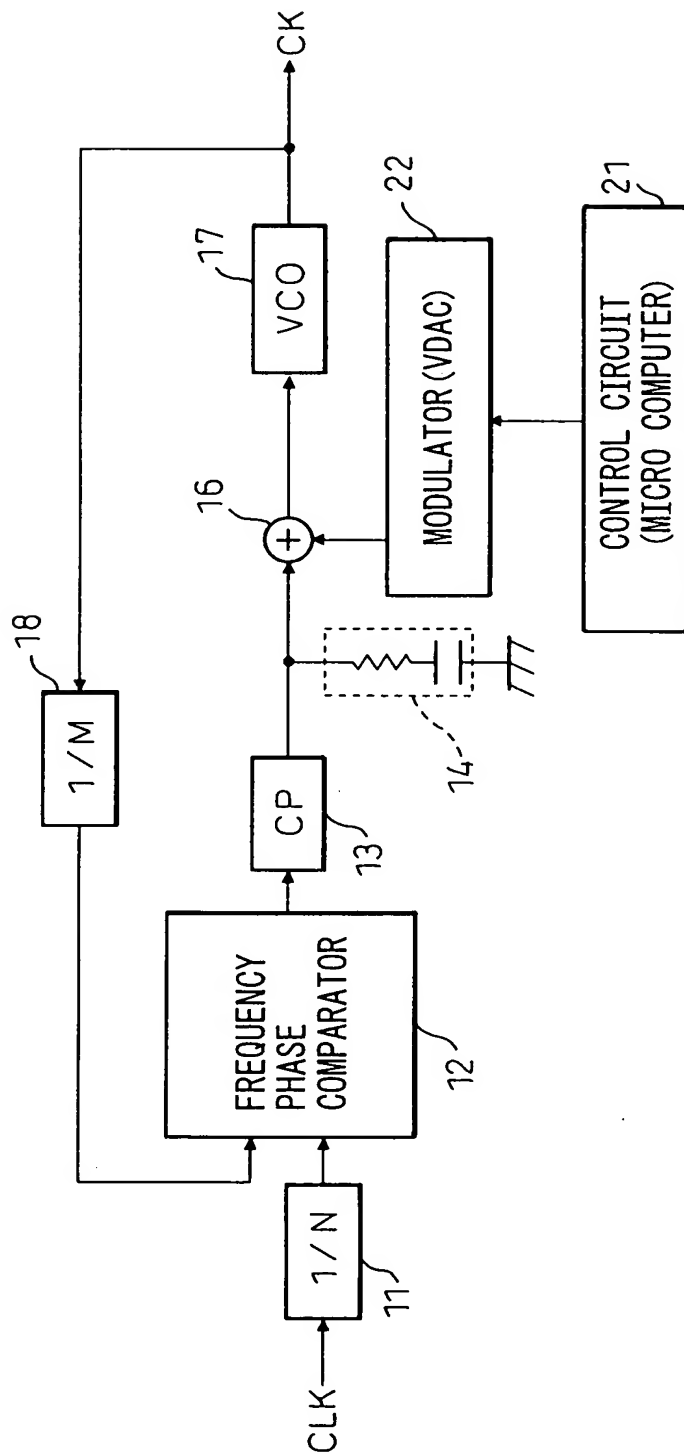


FIG. 9

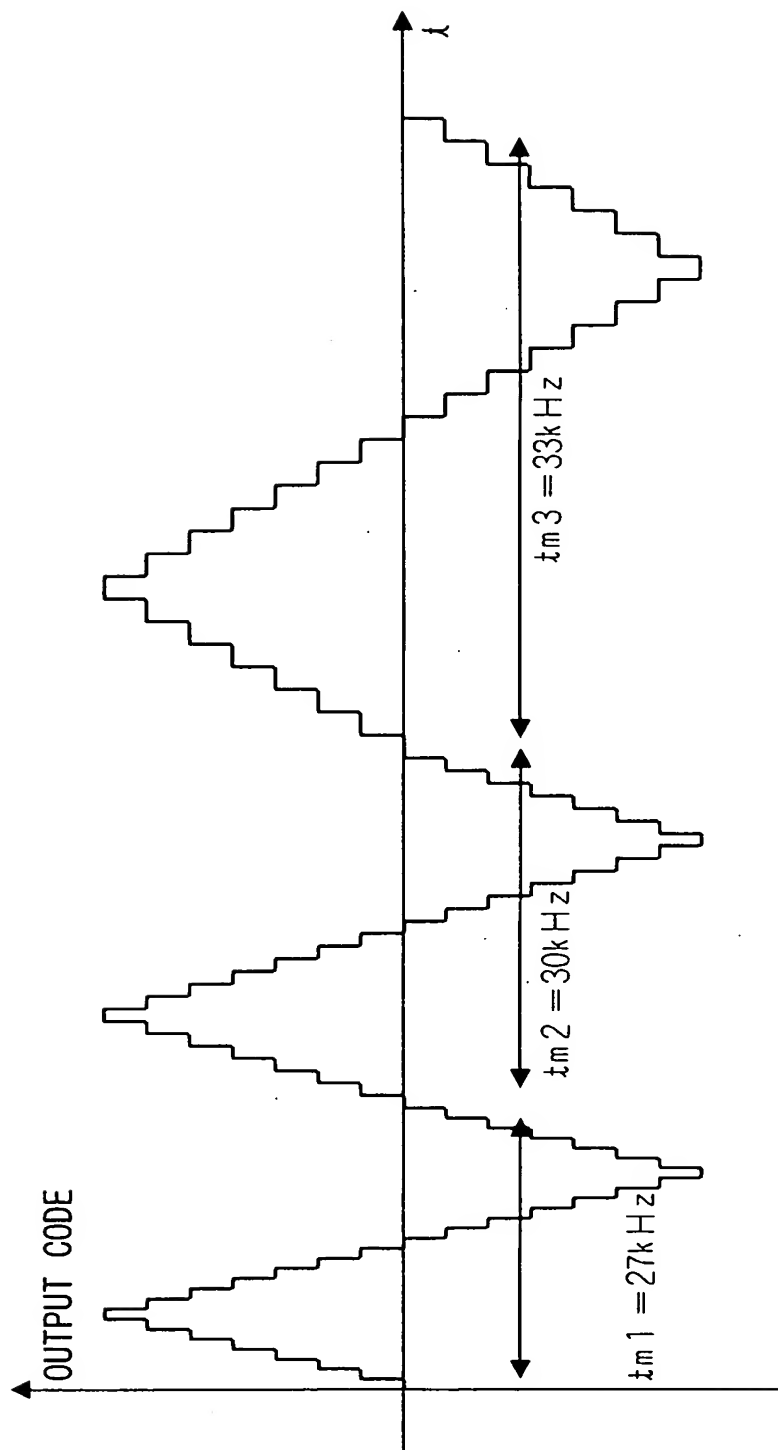
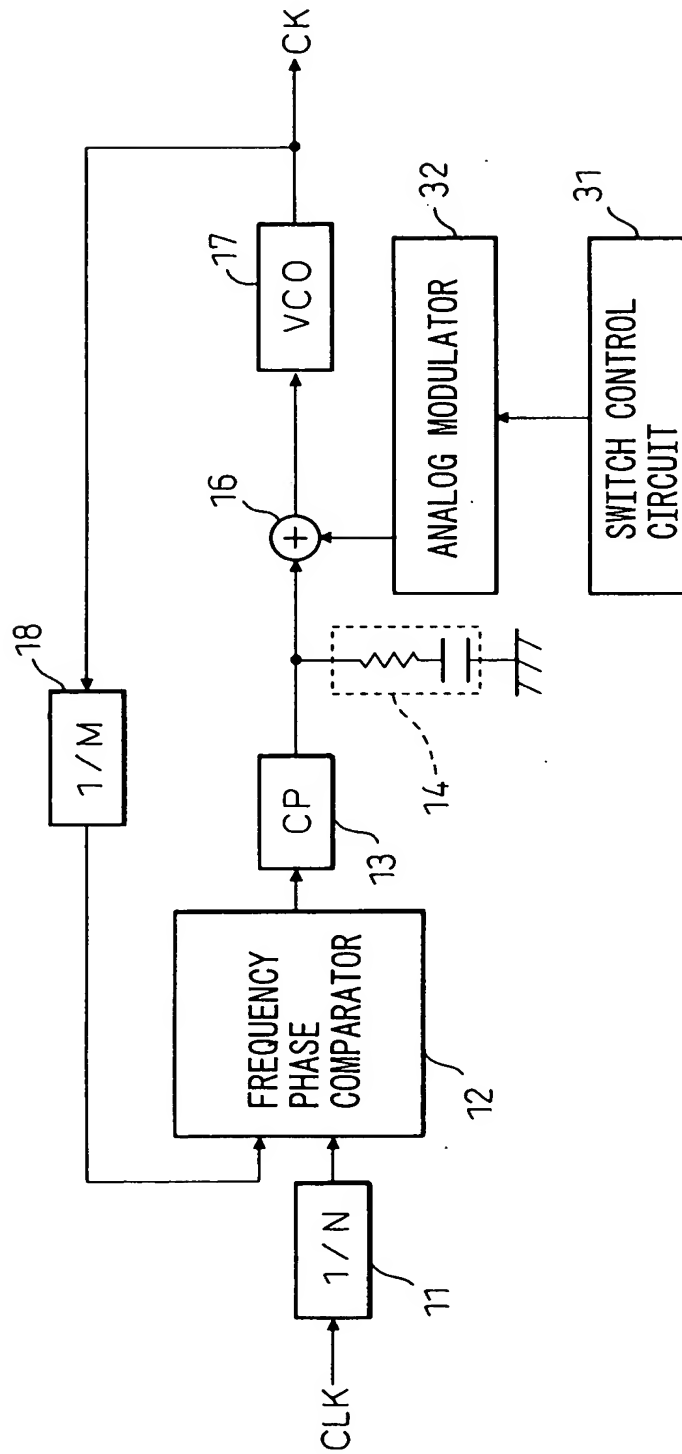


FIG.10



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FIG.11

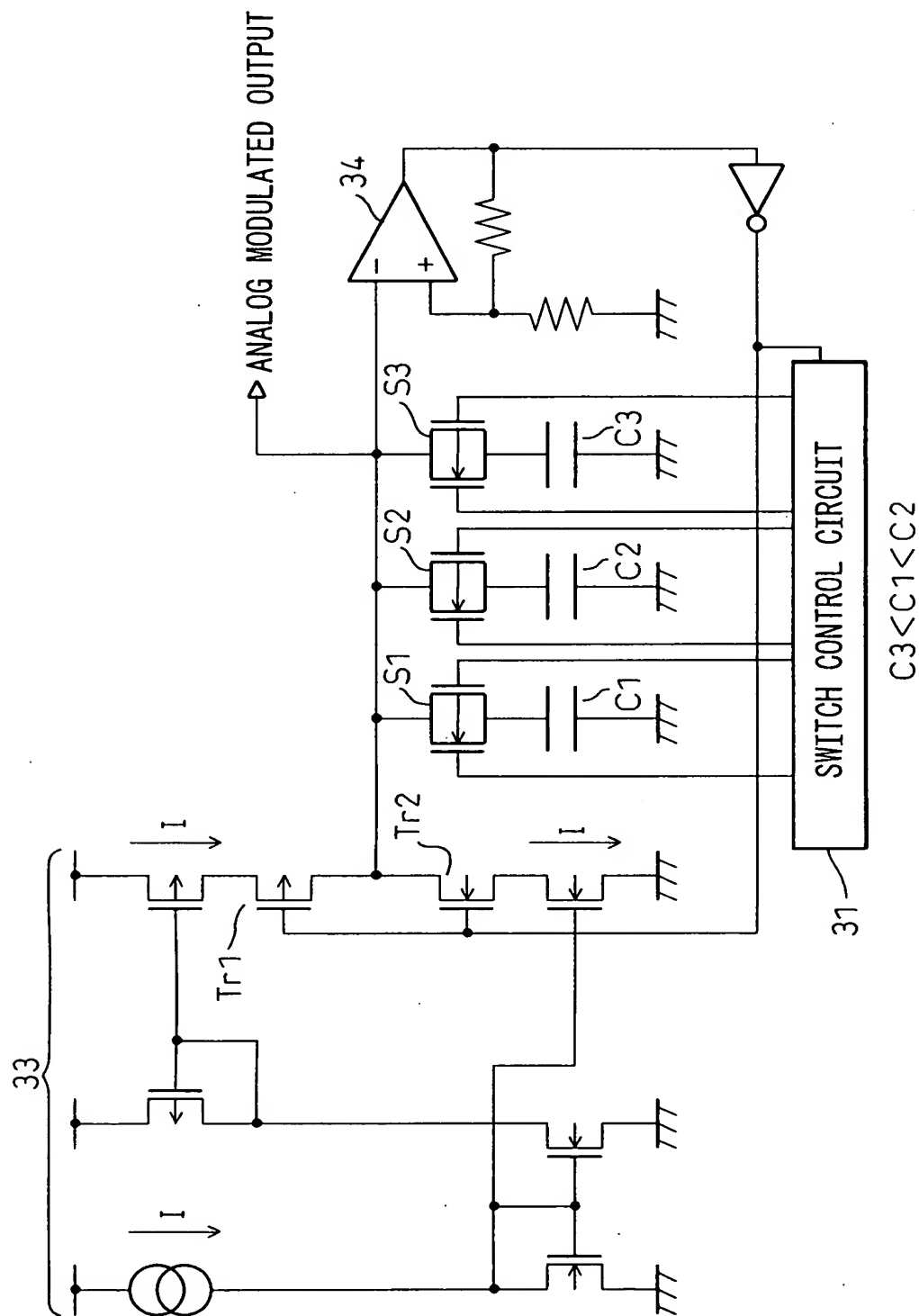
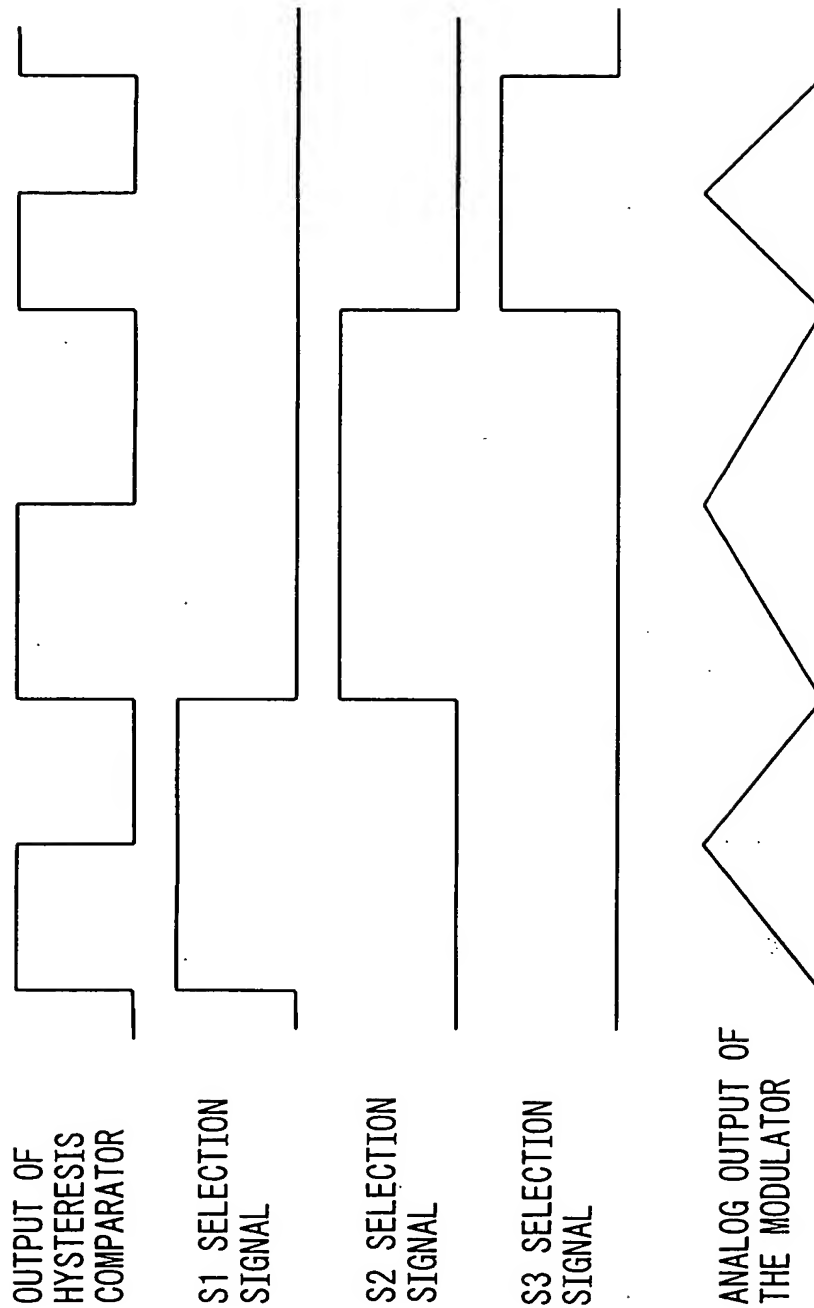
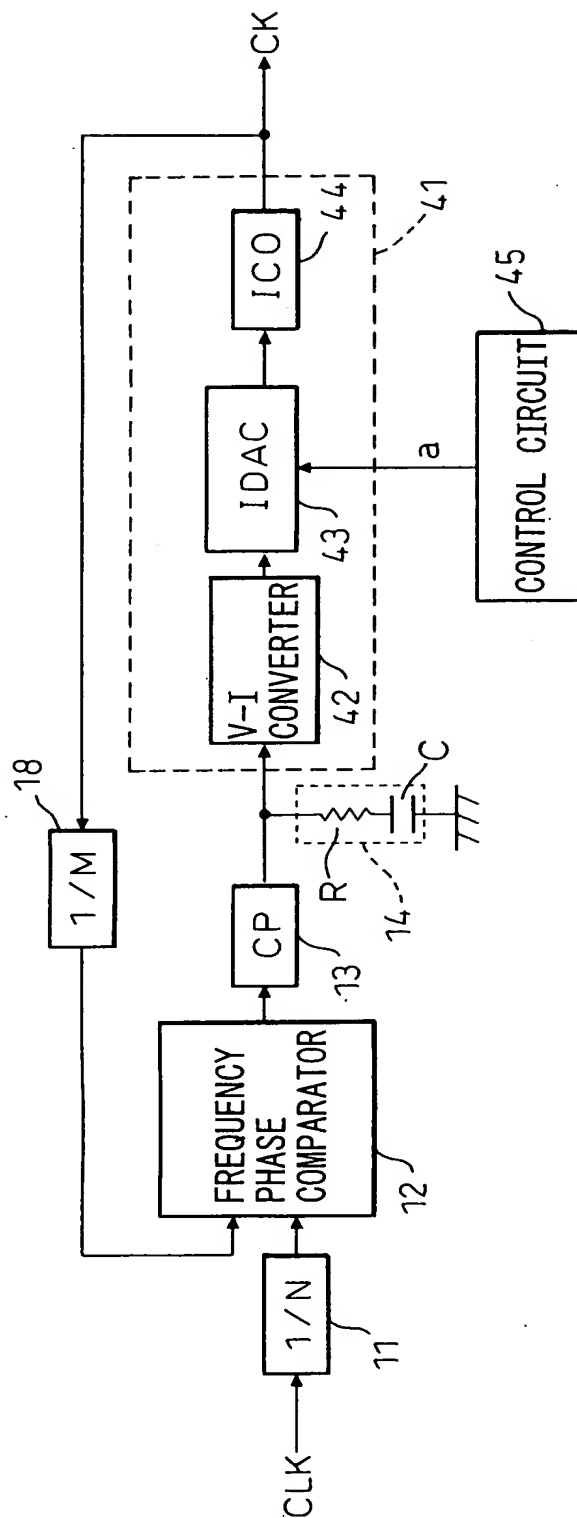


FIG.12



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FIG.13



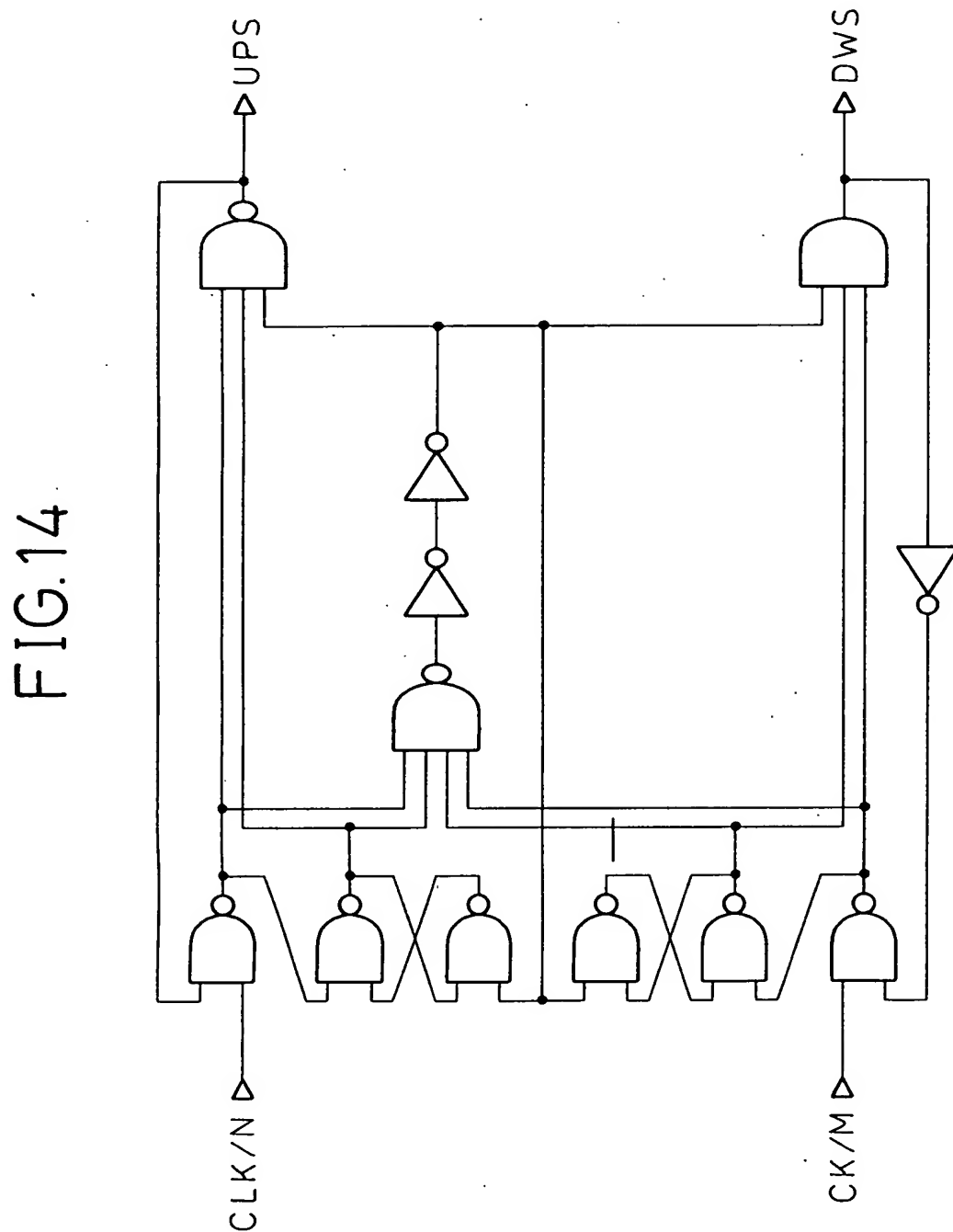


FIG.15

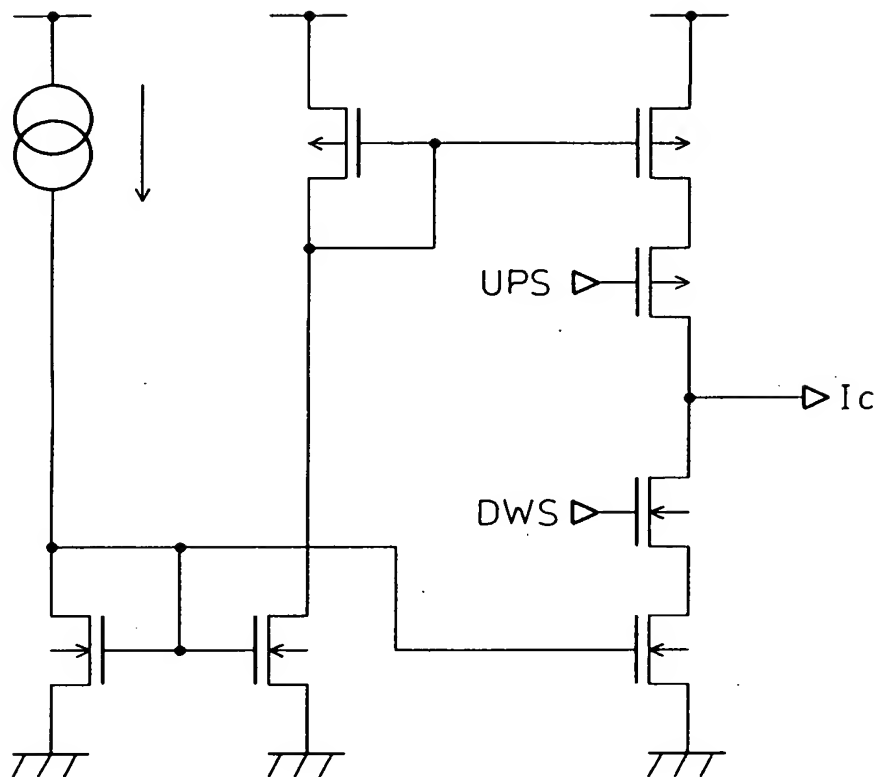


FIG.16

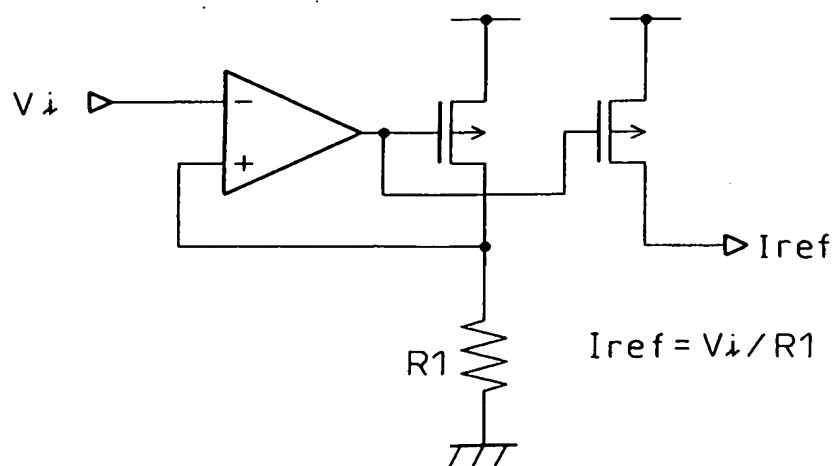


FIG. 17

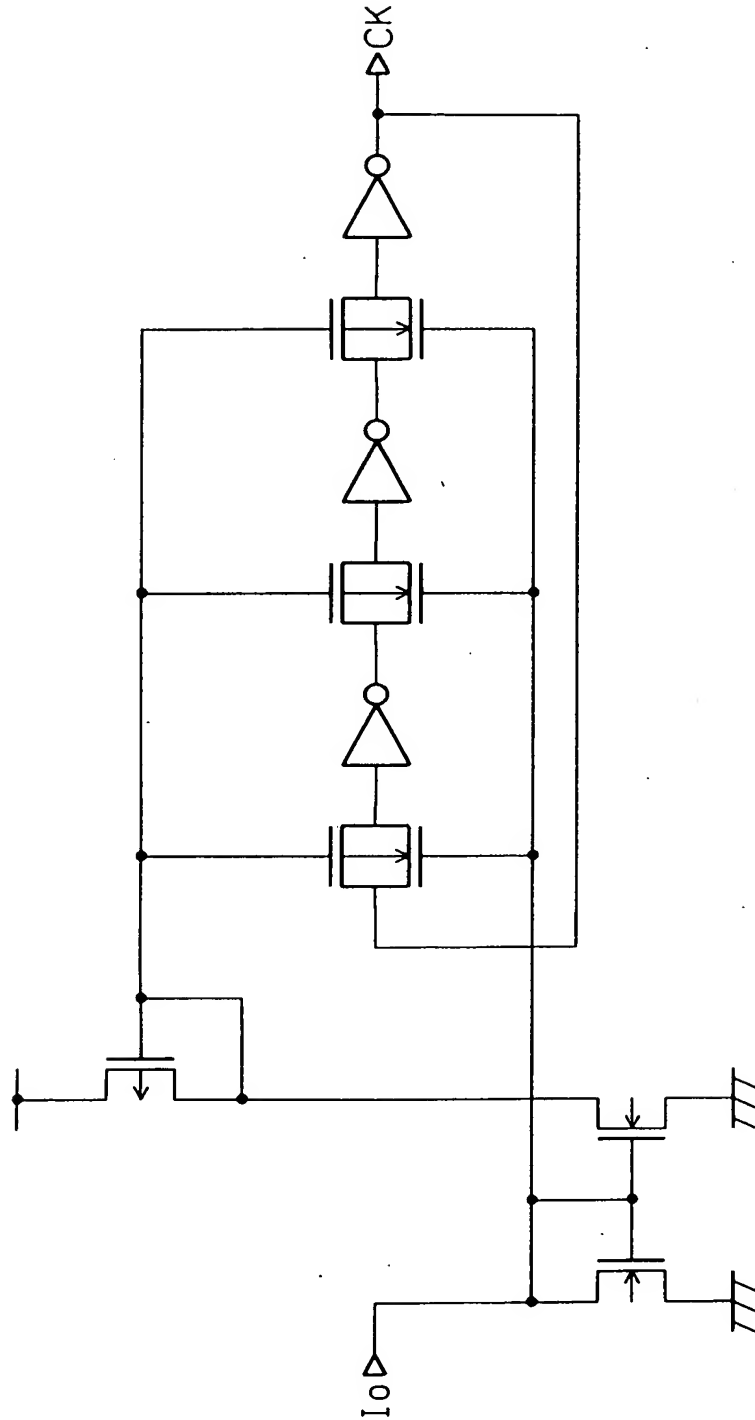


FIG.18

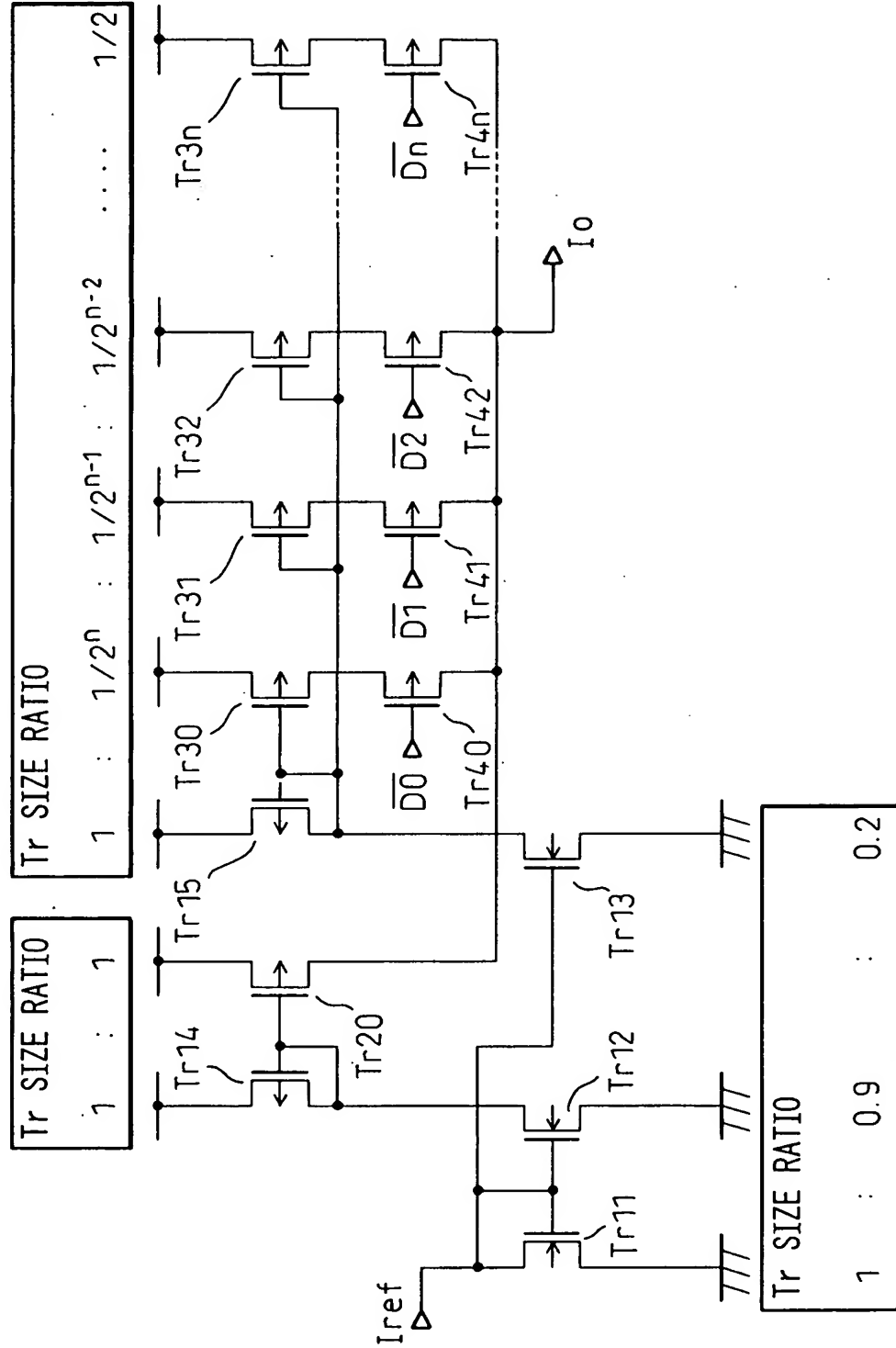


FIG. 19

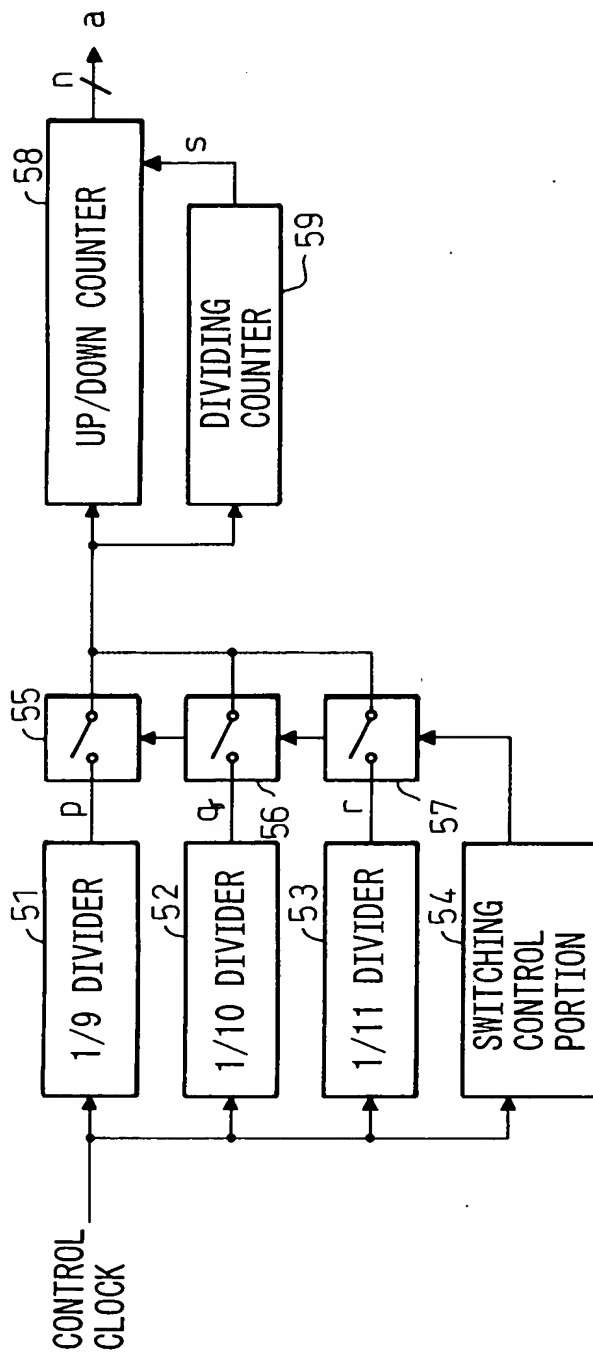


FIG. 20

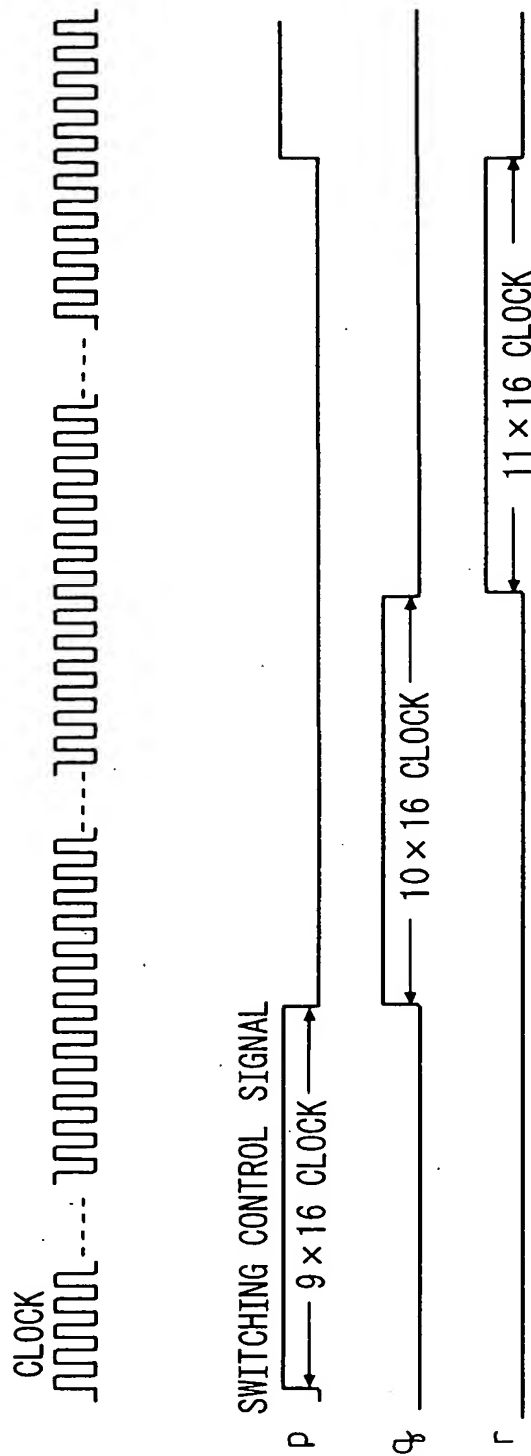


FIG. 21

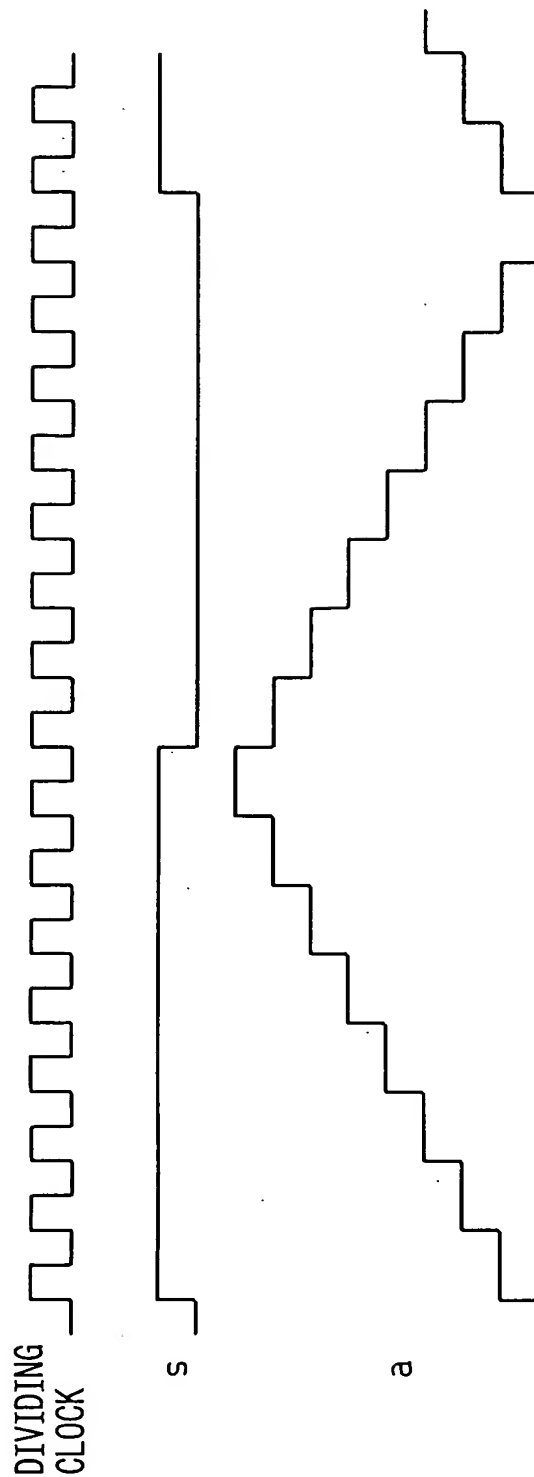


FIG. 22

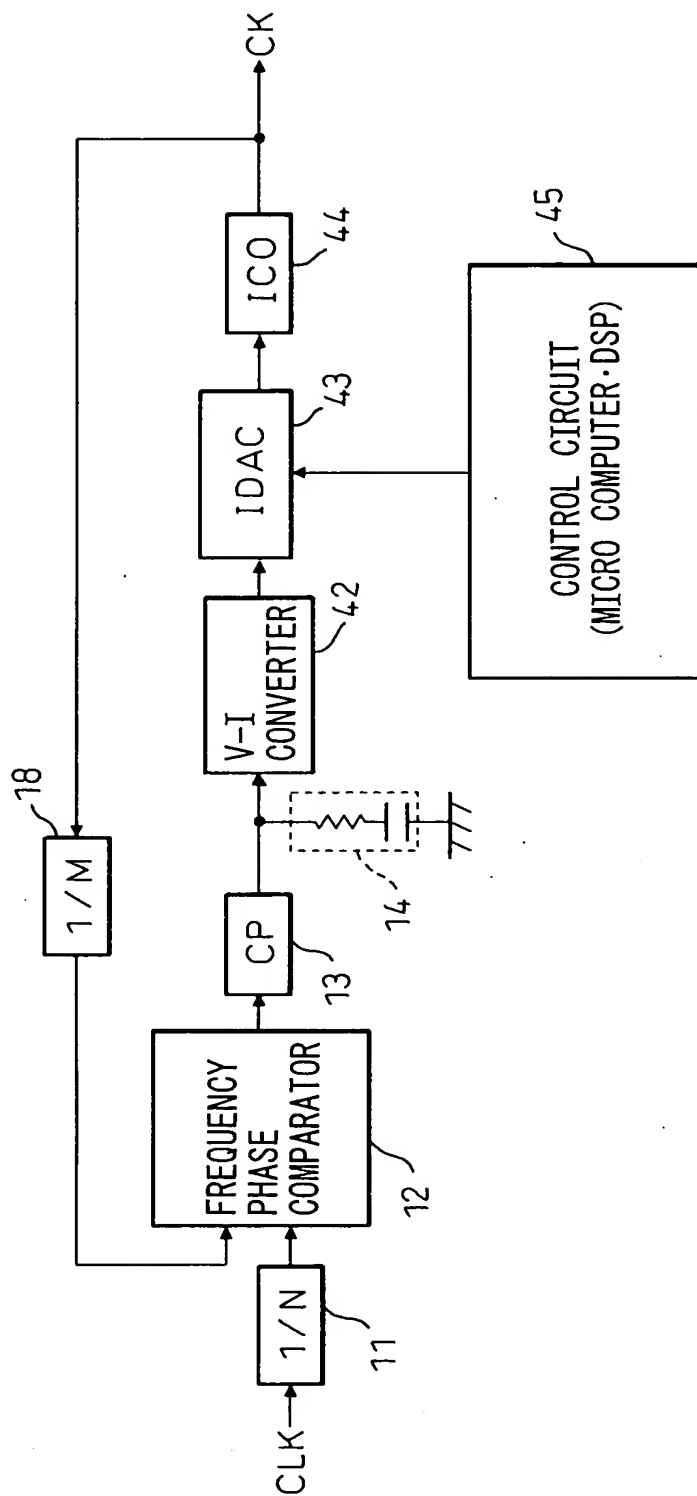


FIG. 23

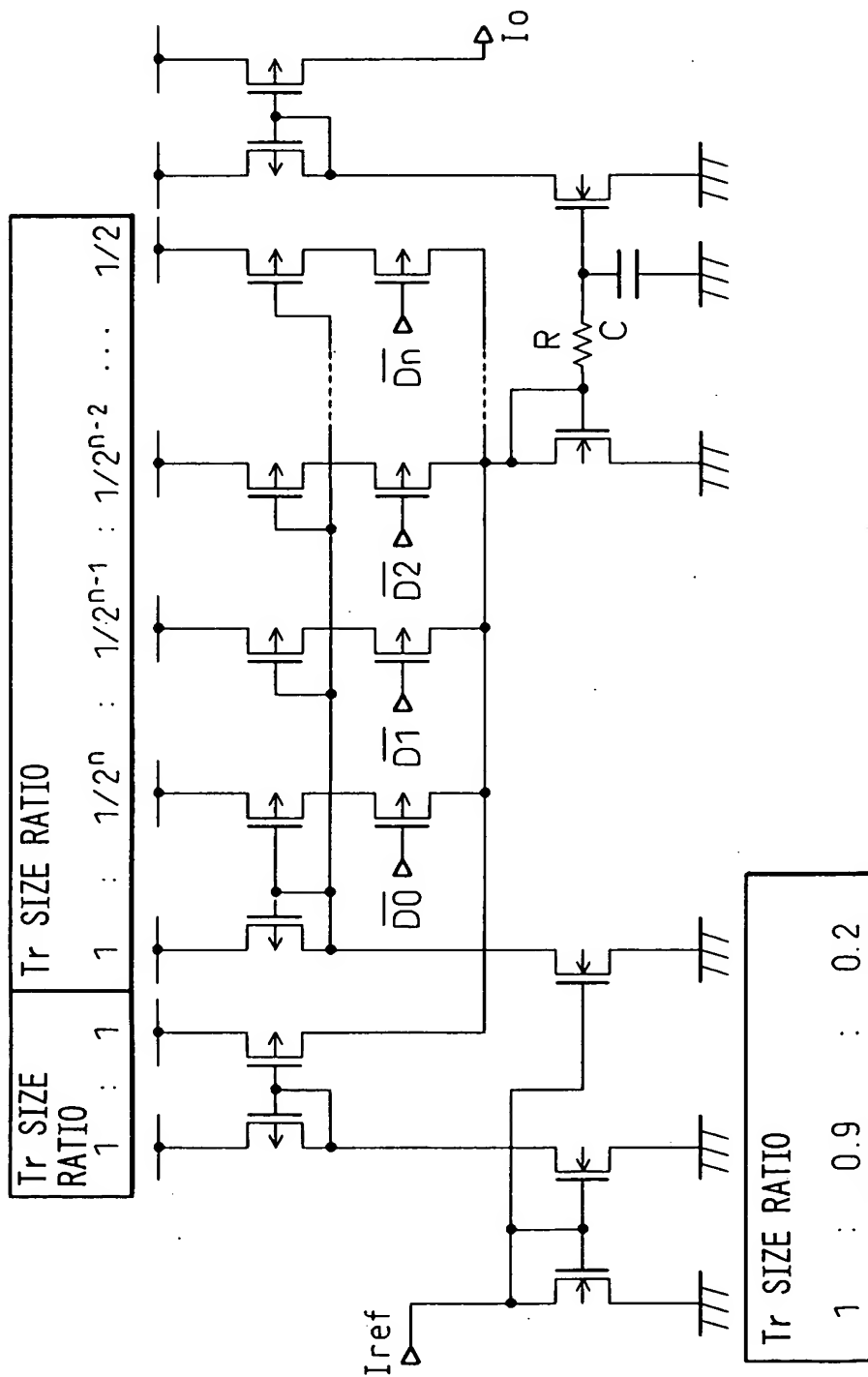


FIG. 24

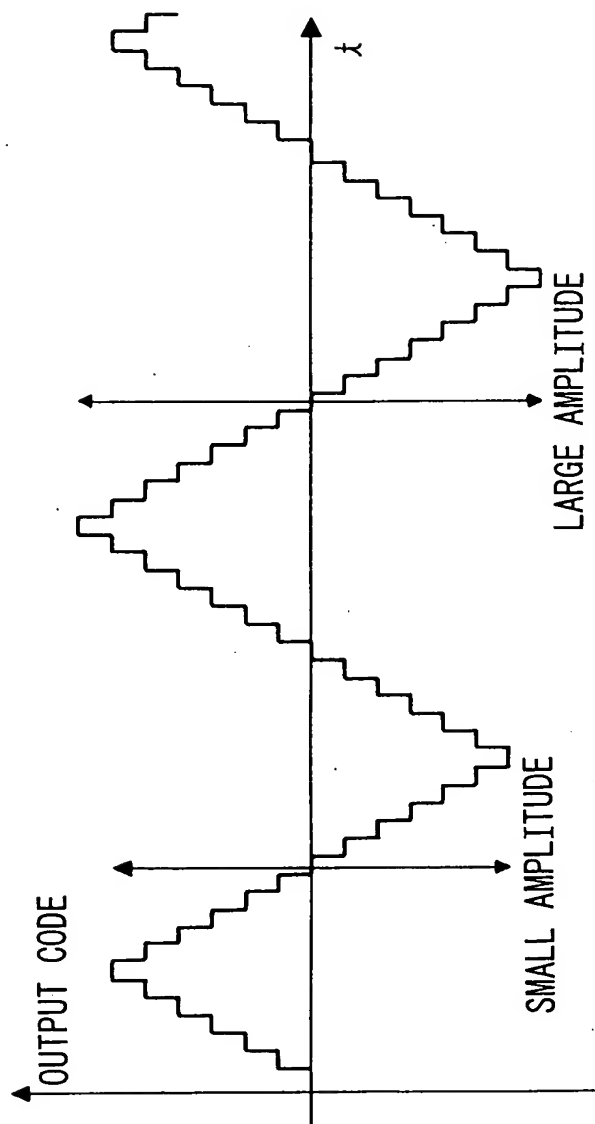


FIG. 25A

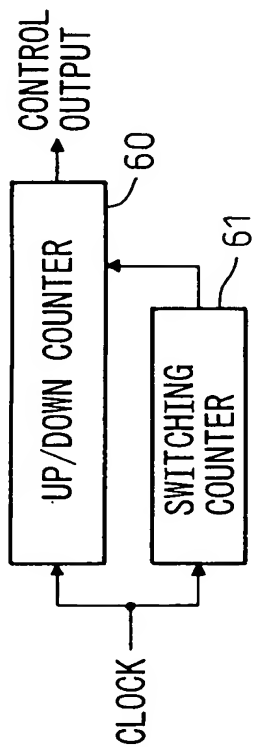


FIG. 25B

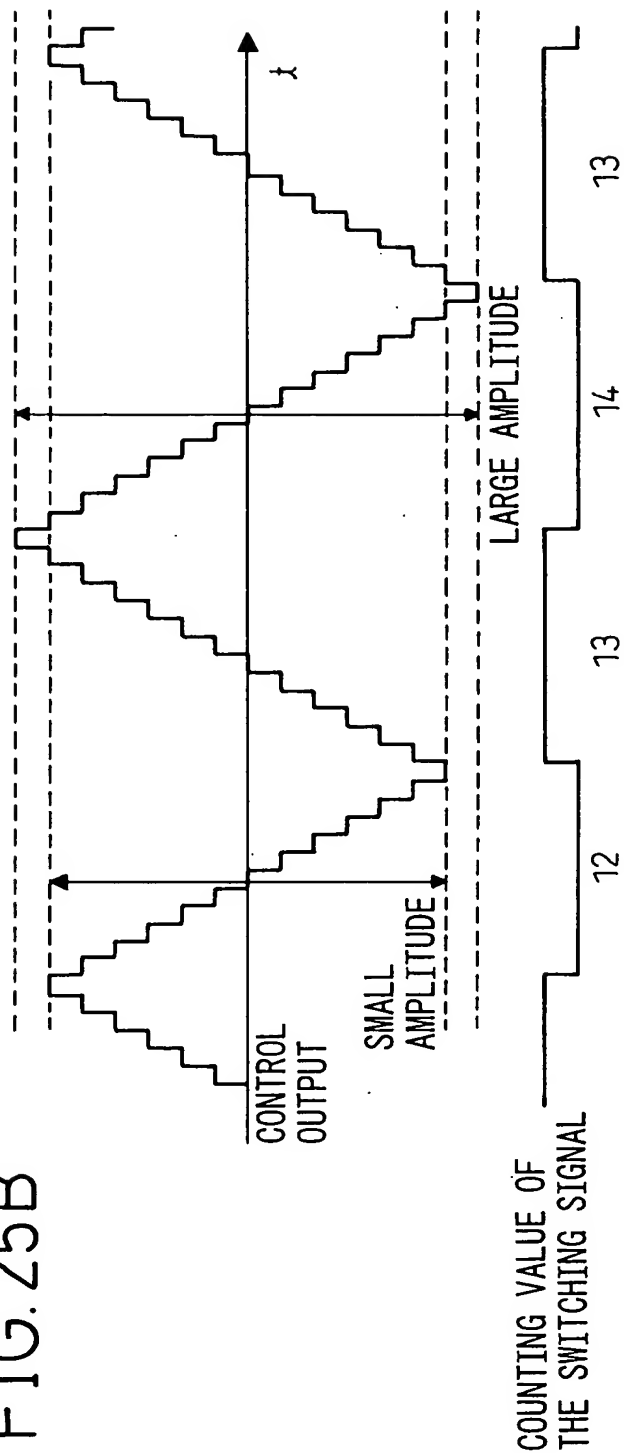


FIG. 26A

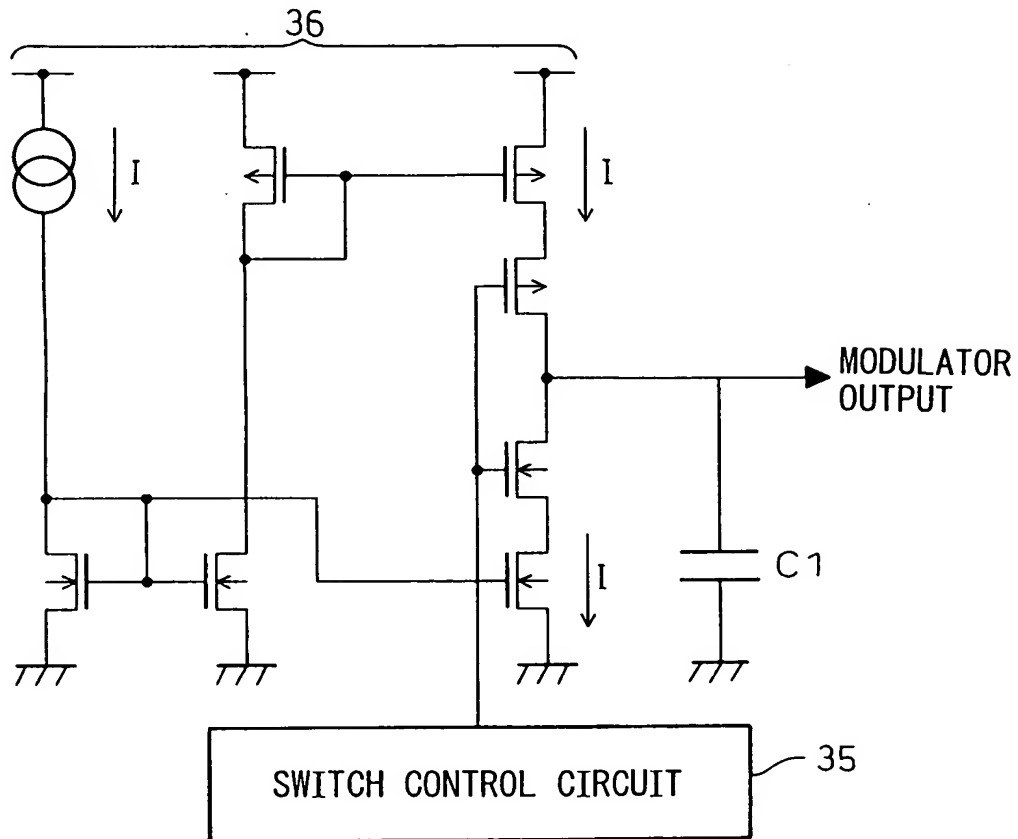


FIG. 26B

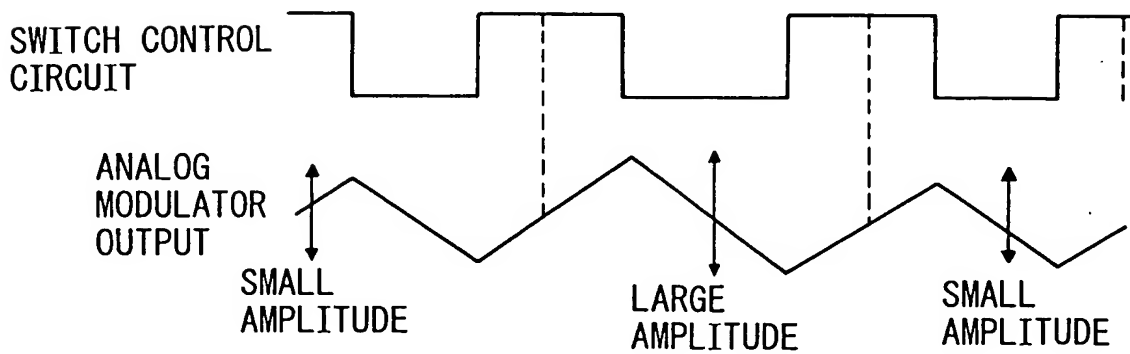


FIG. 27

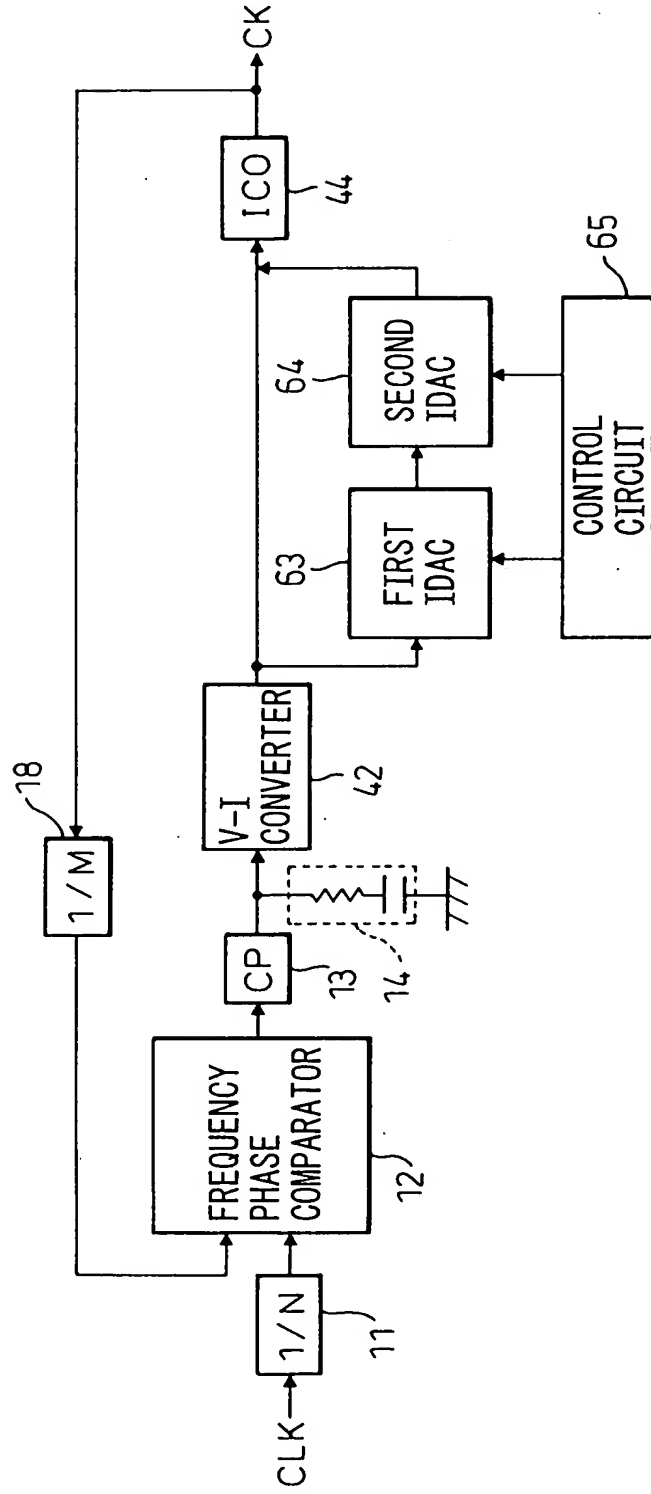


FIG. 28

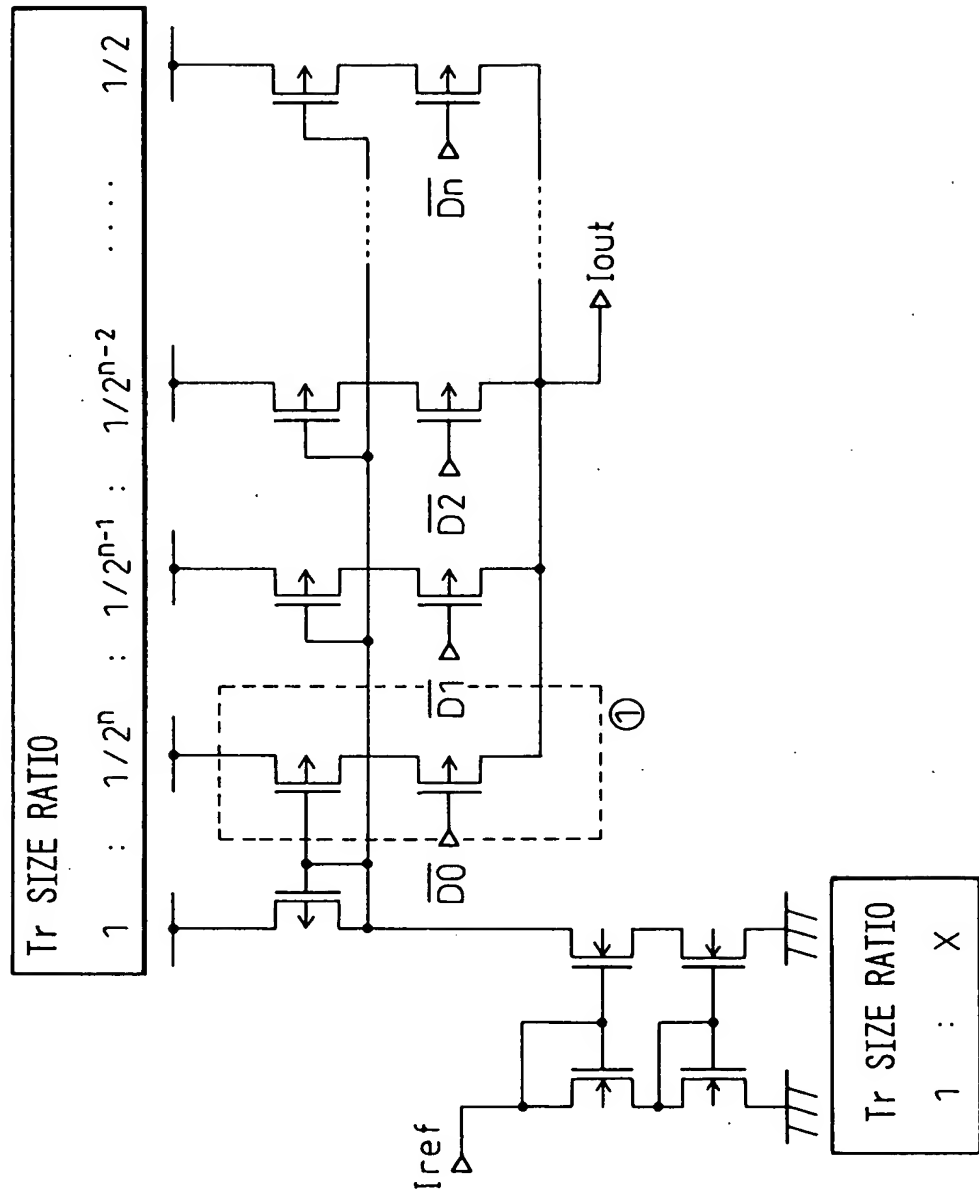


FIG. 29

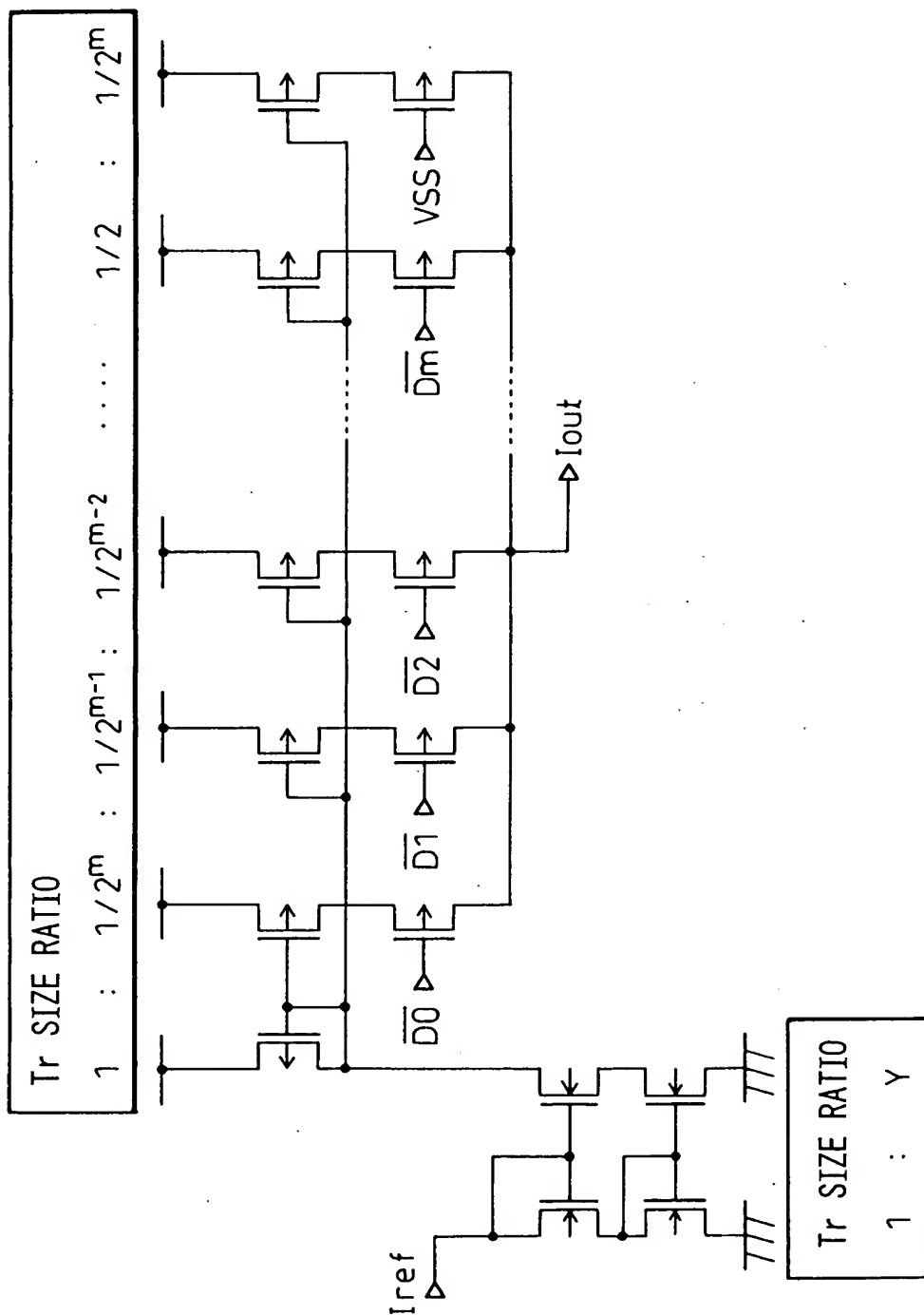


FIG.30A

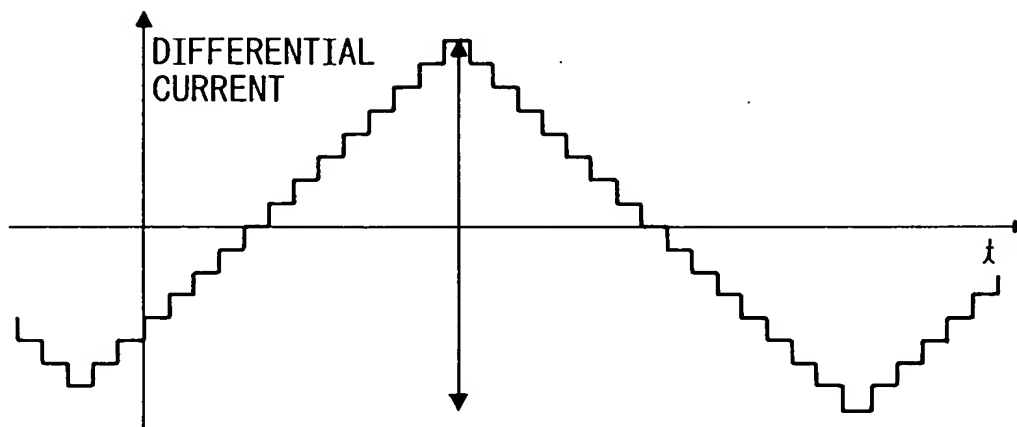


FIG.30B

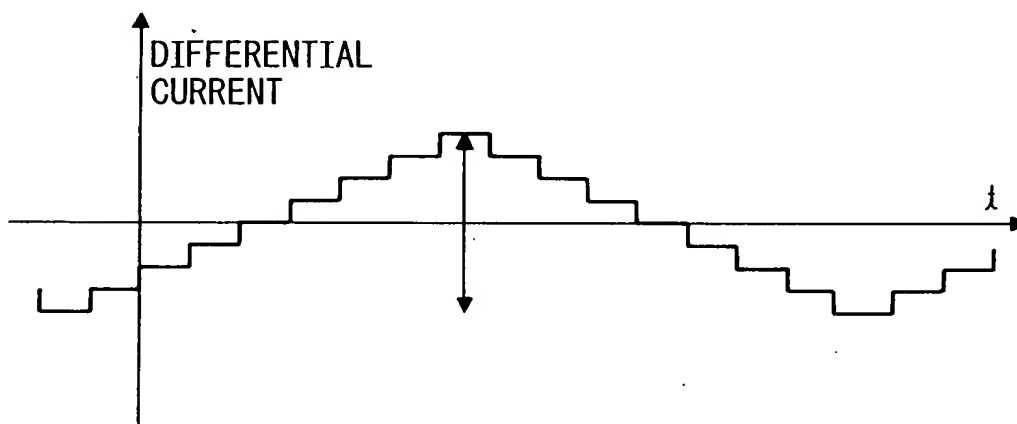


FIG.30C

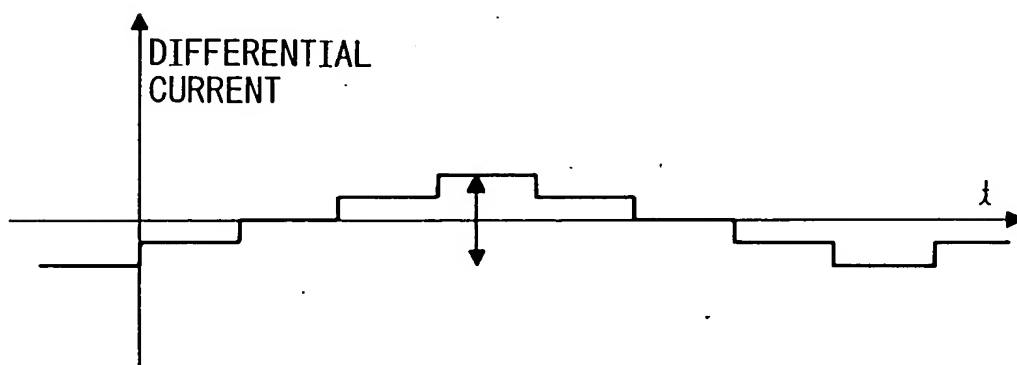


FIG. 31A

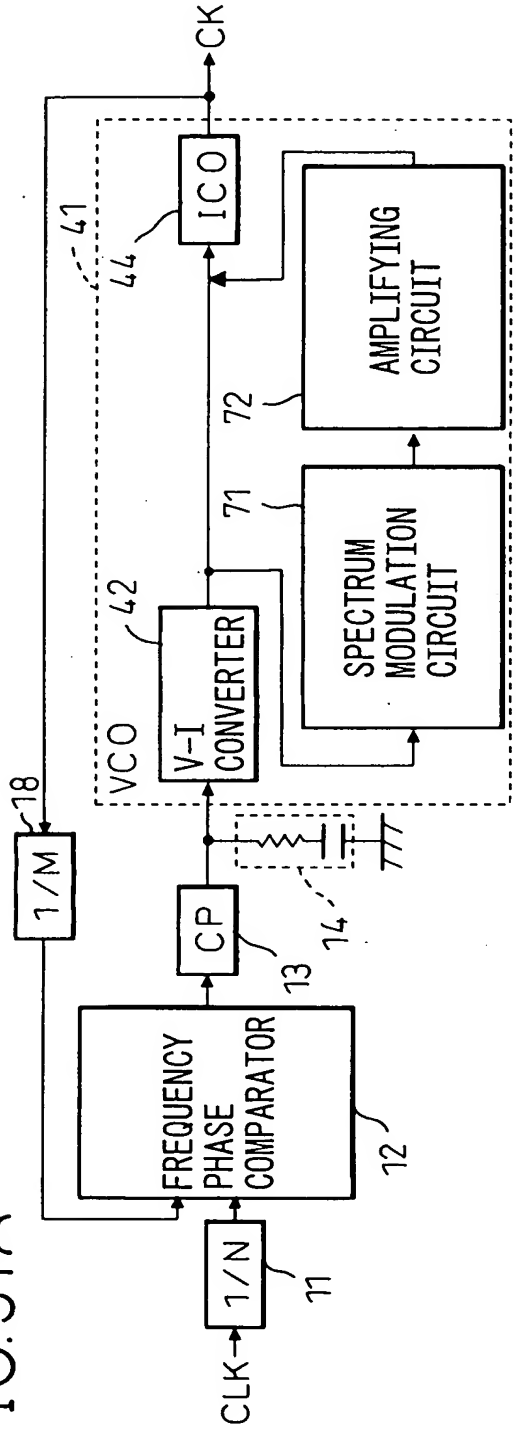


FIG. 31B

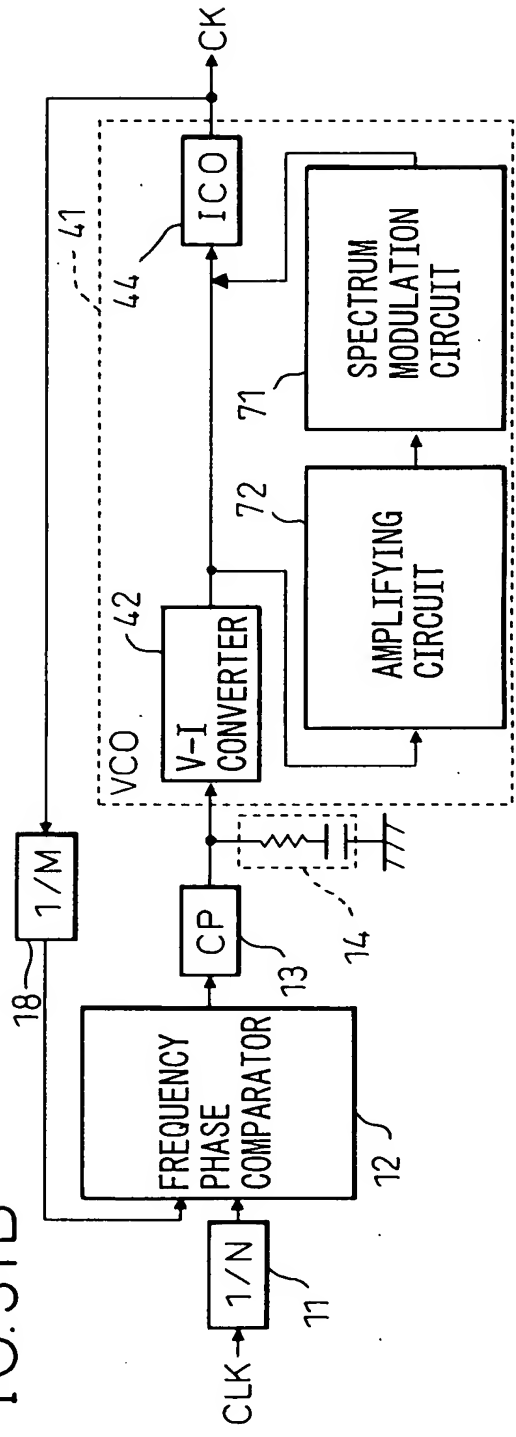


FIG. 32A

AMPLITUDE A

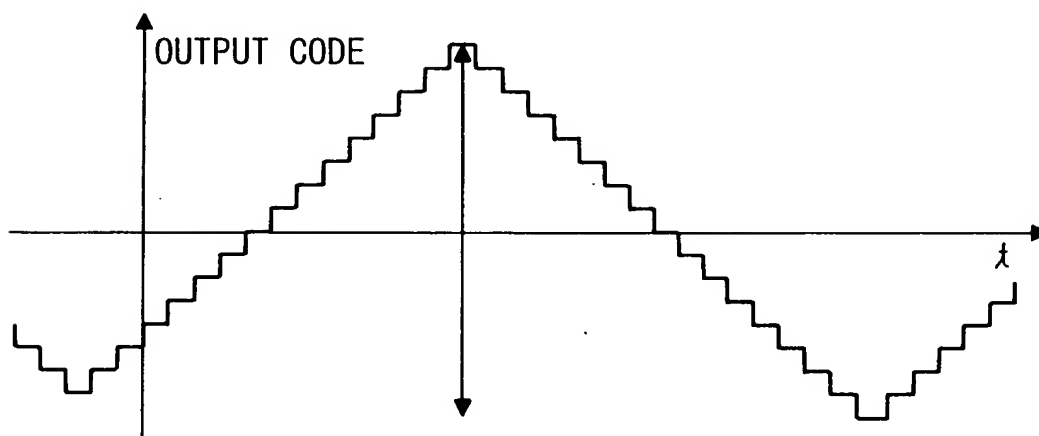
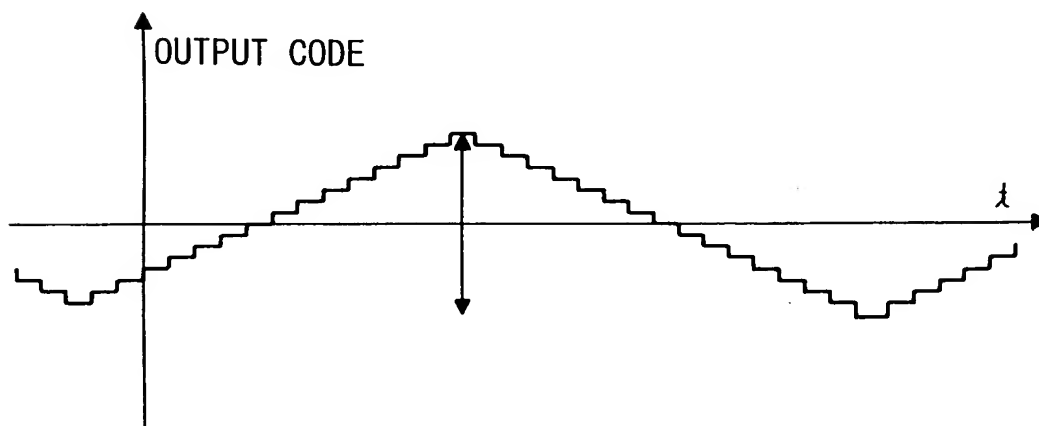


FIG. 32B

AMPLITUDE A k/m



[illegible]

FIG. 34A

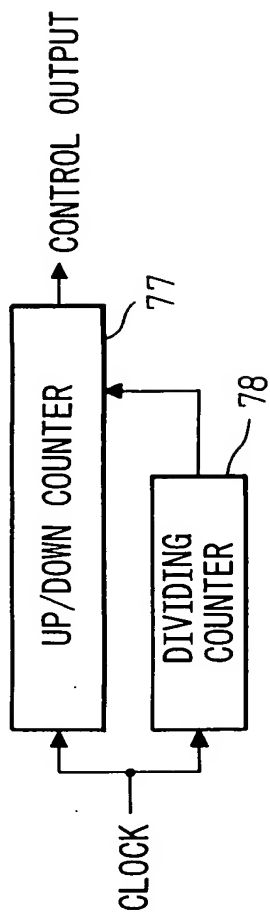


FIG. 34B

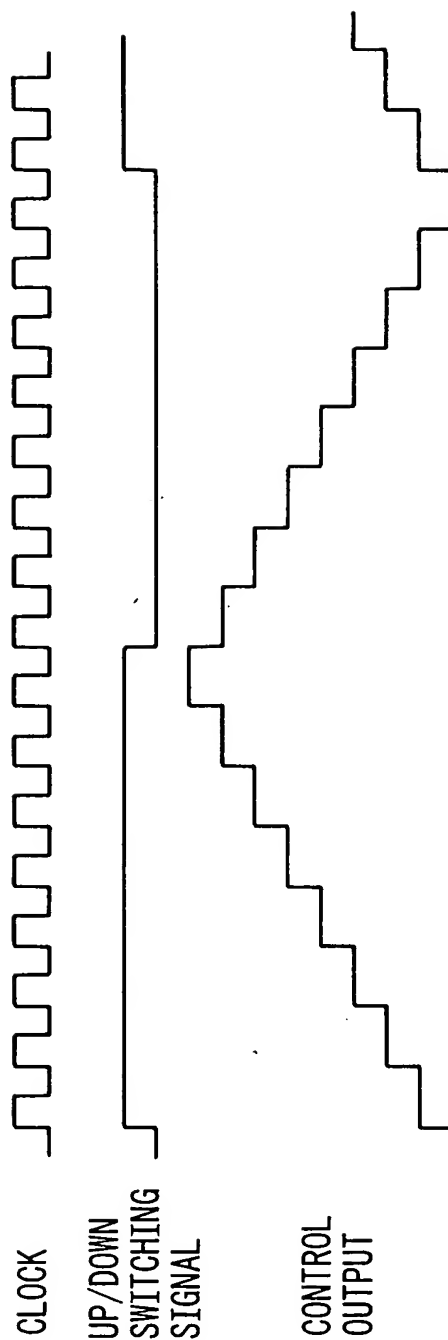


FIG.35

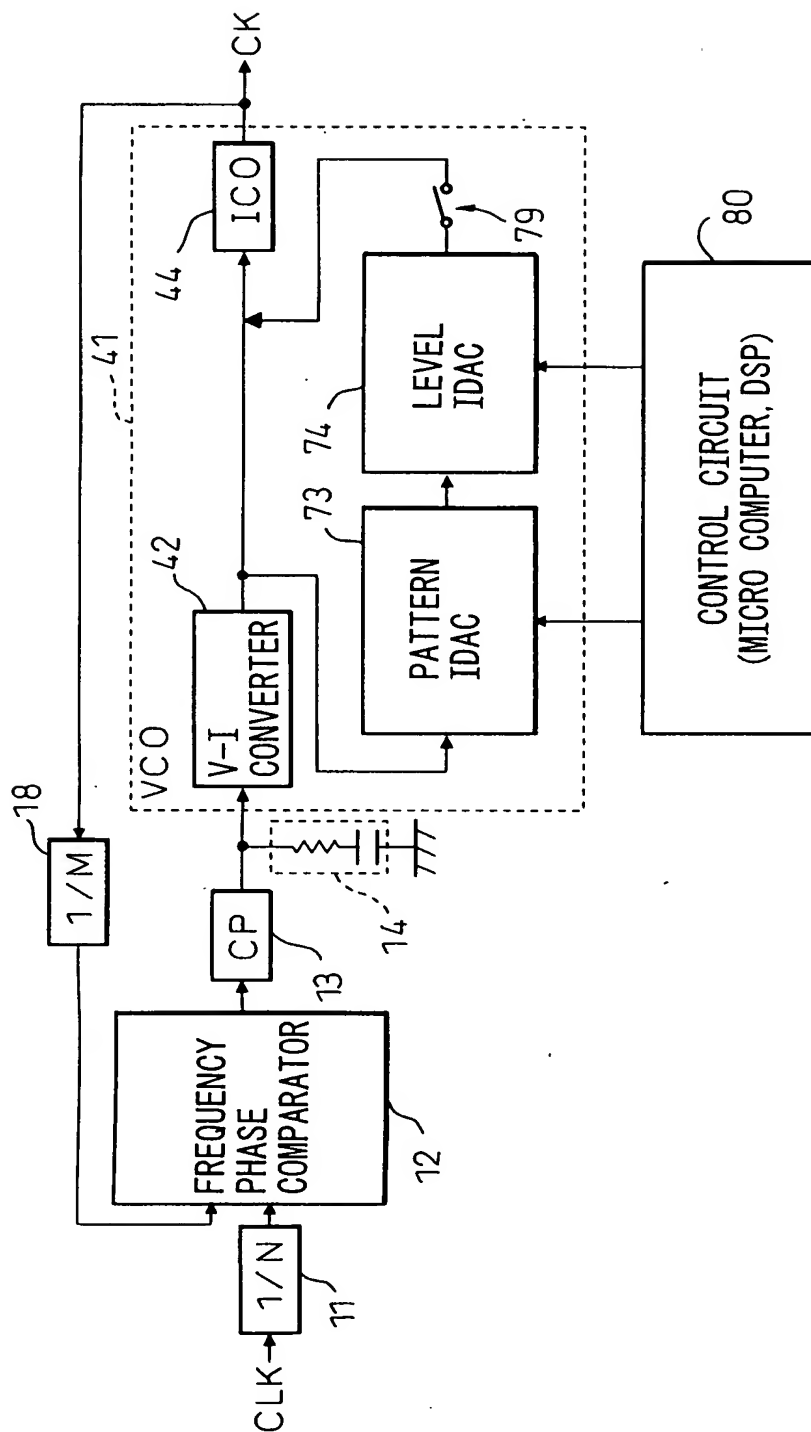


FIG. 36A

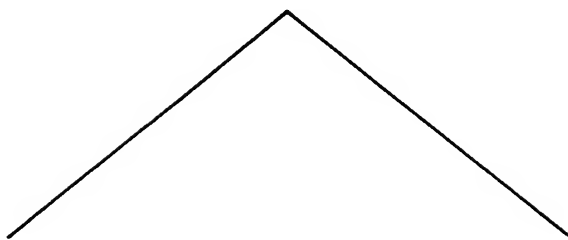


FIG. 36B

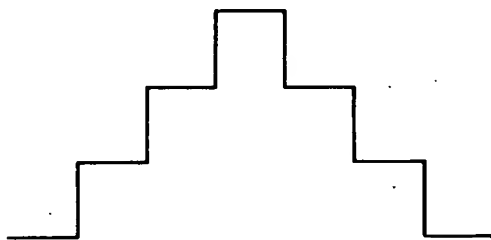


FIG. 36C

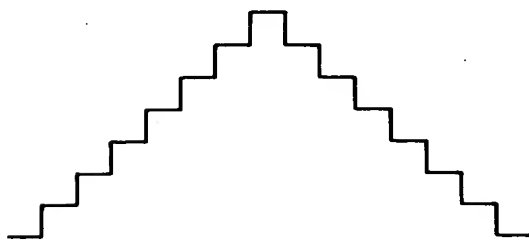


FIG. 37

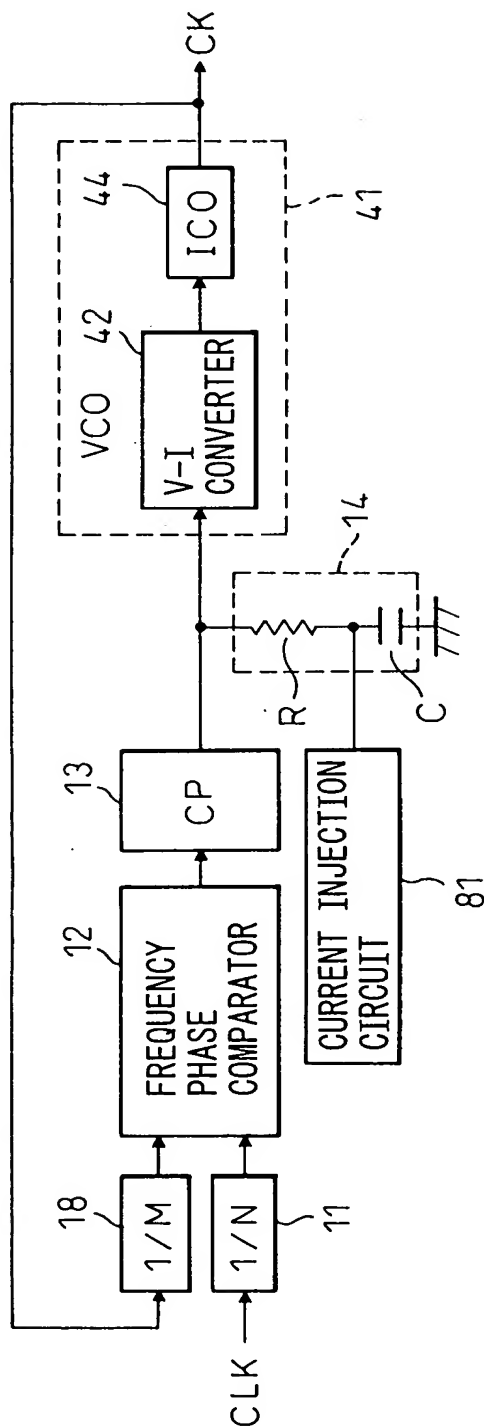


FIG. 38

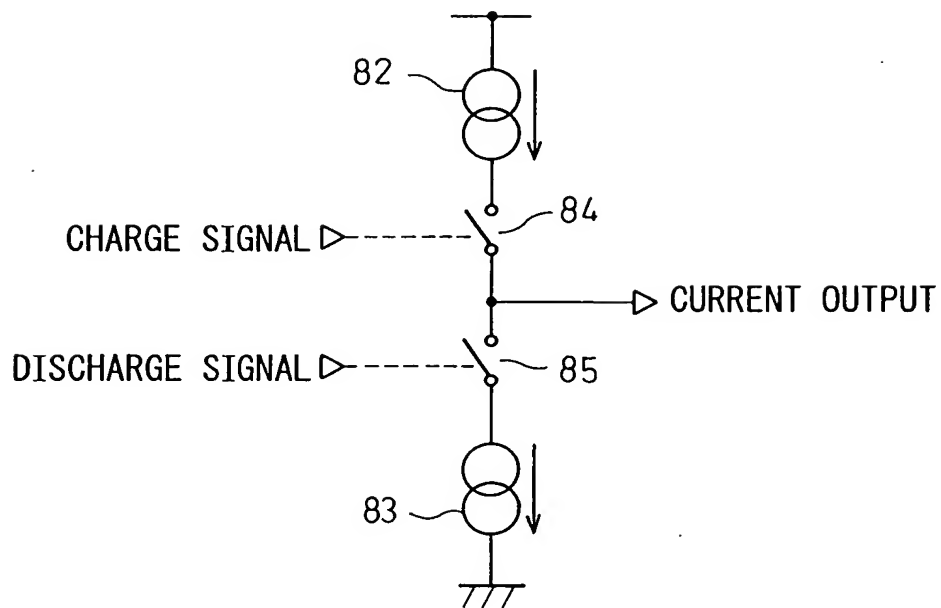


FIG. 39

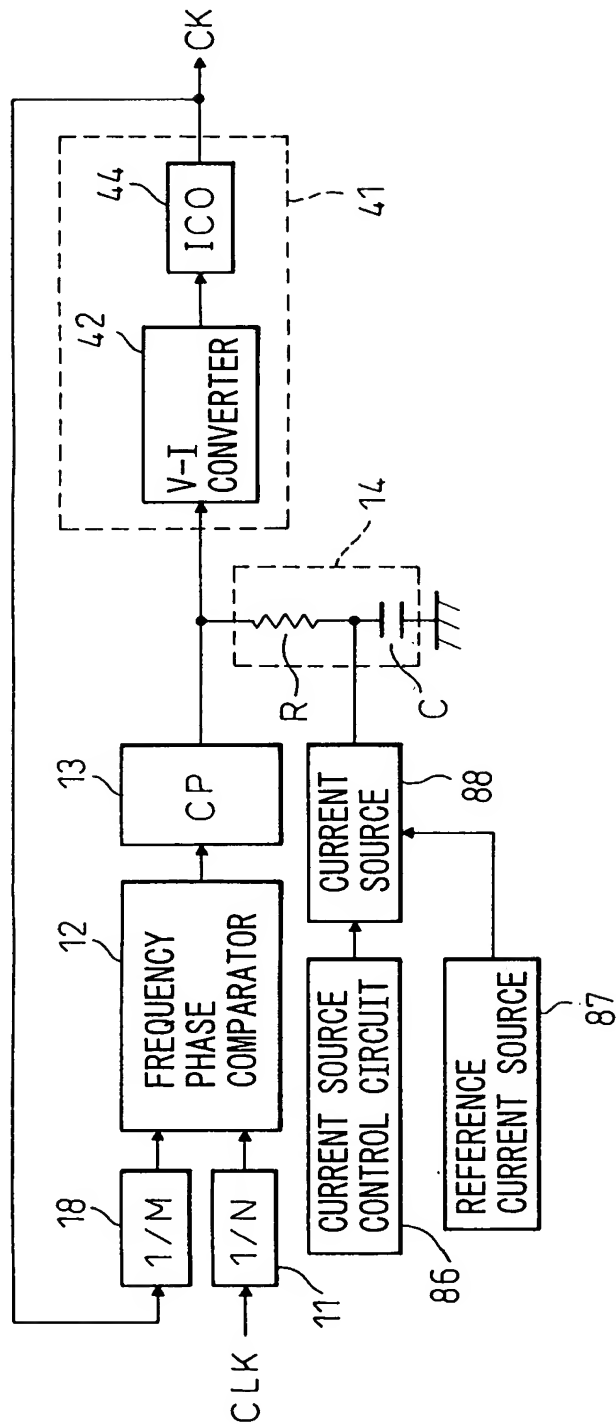


FIG. 40

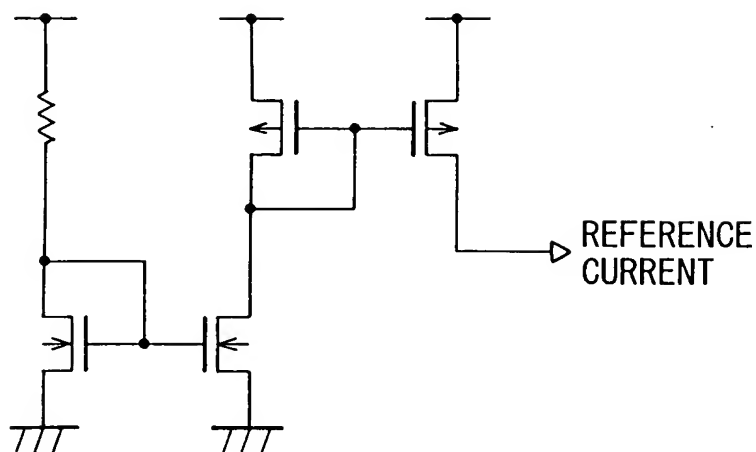
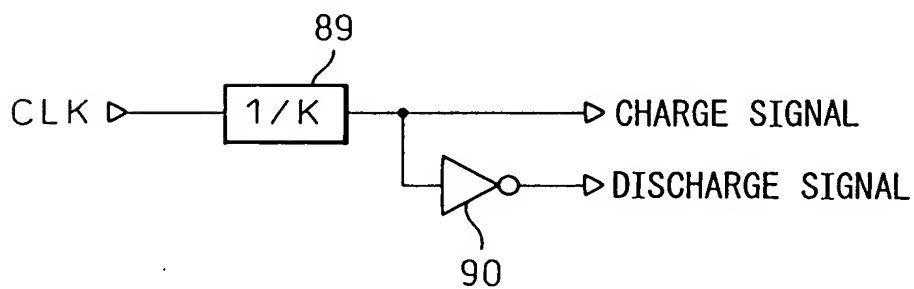


FIG. 41



The circuit diagram (FIG. 7) illustrates a current source circuit. It features a central vertical line representing a common node. On the left side, there are three inputs: 'CHARGE SIGNAL', 'DISCHARGE SIGNAL', and 'REFERENCE CURRENT'. The 'CHARGE SIGNAL' is inverted and connected to the gate of transistor Tr76. The 'DISCHARGE SIGNAL' is connected to the gate of transistor Tr77. The 'REFERENCE CURRENT' is connected to the gates of transistors Tr71 and Tr72. Transistors Tr73 and Tr74 are connected to the common node and have their gates connected to a common point. Transistors Tr75, Tr76, and Tr77 are connected to the common node and have their gates connected to the 'DISCHARGE SIGNAL' input. The output of the circuit is labeled 'CURRENT OUTPUT' and is connected to the common node. The circuit is powered by a supply voltage and ground.

FIG. 43A

CHARGE SIGNAL

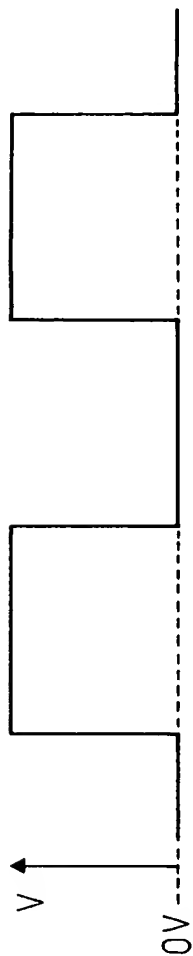


FIG. 43B

DISCHARGE SIGNAL

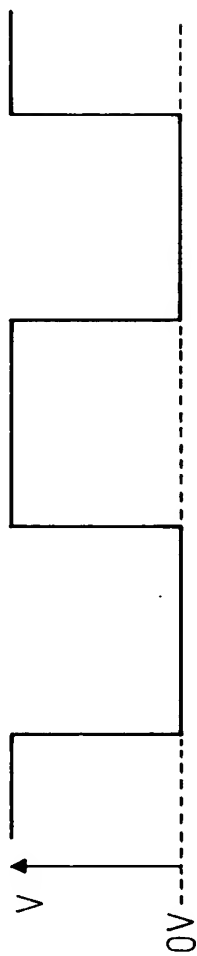


FIG. 43C

CURRENT OF THE
 CURRENT SOURCE

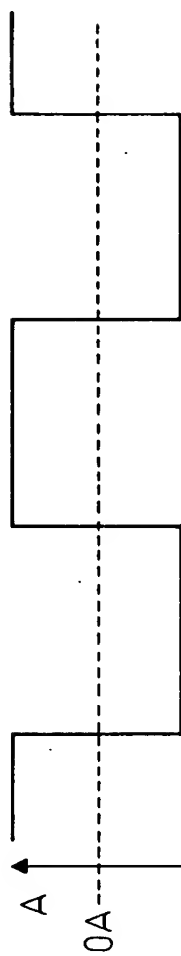


FIG. 43D

VOLTAGE OF A NODE
 BETWEEN A RESISTOR
 AND A CAPACITOR OF
 A LOOP-FILTER
 (VCO CONTROL
 VOLTAGE)

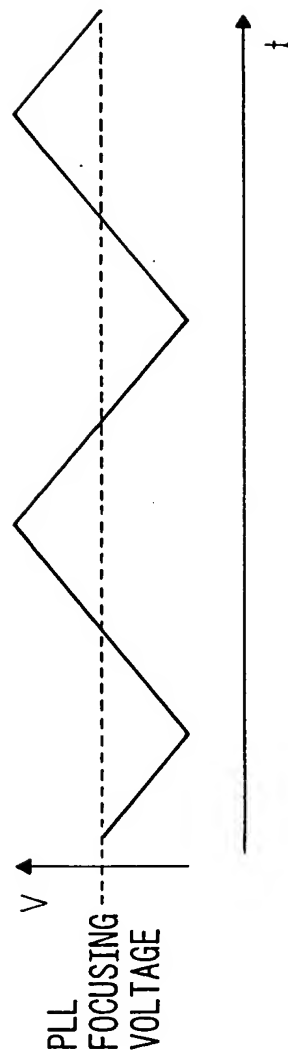
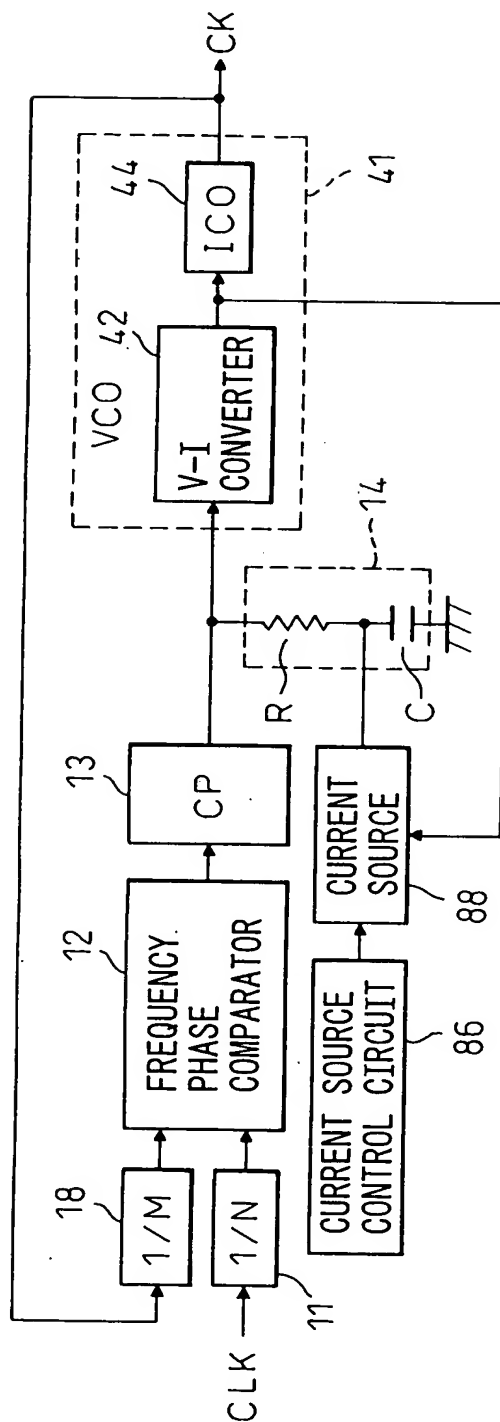


FIG. 44



The diagram shows a PLL circuit. An input signal **CLK** is divided by **1/N** (block 11) and **1/M** (block 18). The output of **1/M** is fed into a **FREQUENCY PHASE COMPARATOR** (block 12). The output of the comparator is fed into a **CP** (Charge Pump, block 13). The output of the CP is connected to a node that branches to a **V-I CONVERTER** (block 42) and a parallel combination of a resistor **R** and a capacitor **C** (block 14). The output of the V-I converter is fed into an **ICO** (block 44). The outputs of the V-I converter and the ICO are grouped within a dashed box labeled **VCO 42**. The output of the VCO is fed back to the **1/M** divider and also passes through an **LPF** (Low Pass Filter, block 91) before being fed back to the **CP**. A **CURRENT SOURCE** (block 88) is connected to the node between the CP and the resistor/capacitor network. This current source is controlled by a **CURRENT CONTROL CIRCUIT** (block 86), which receives a control signal from the output of the LPF.

FIG. 46

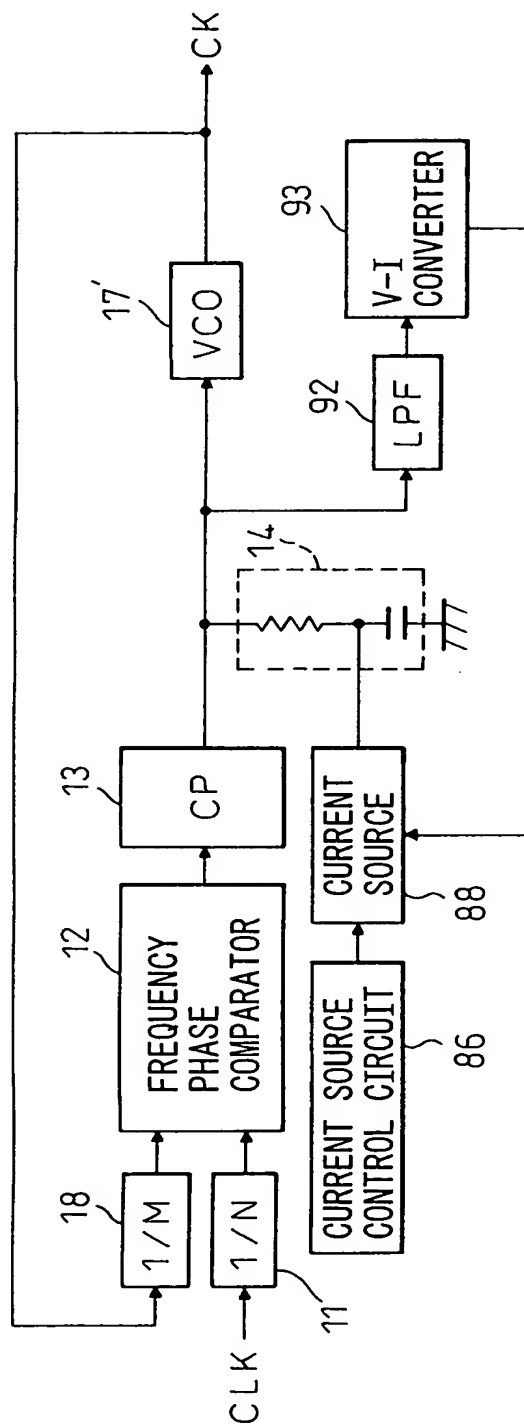


FIG. 47

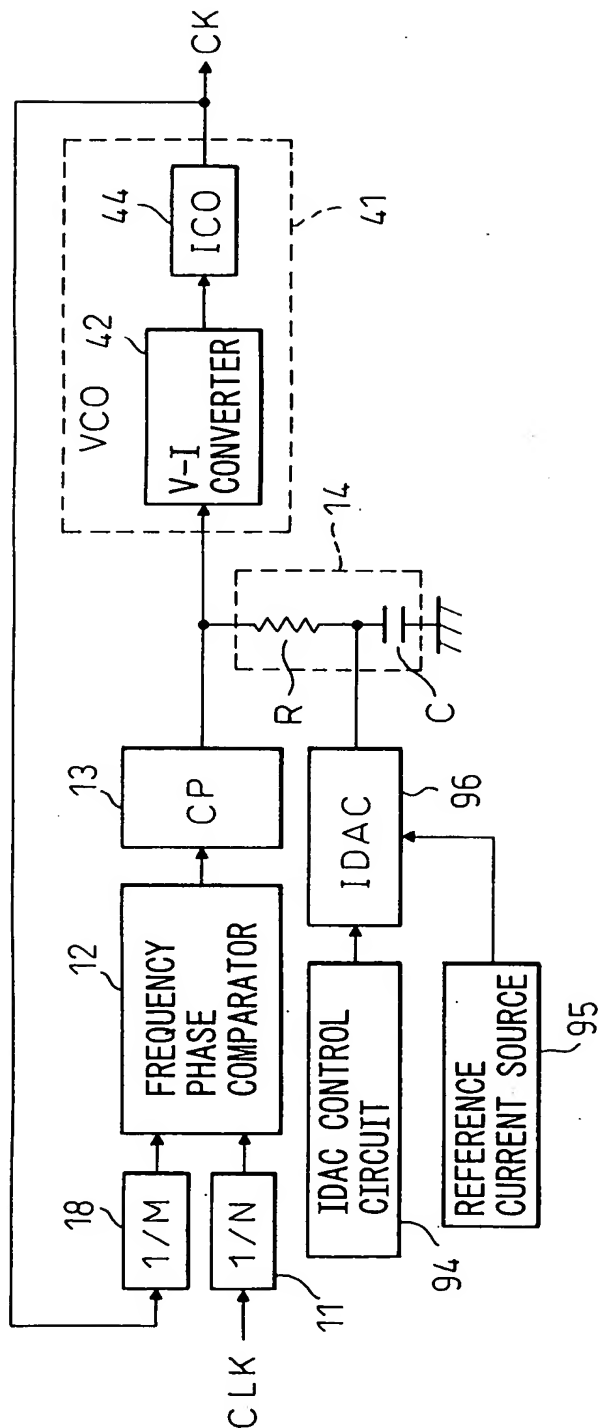


FIG. 48

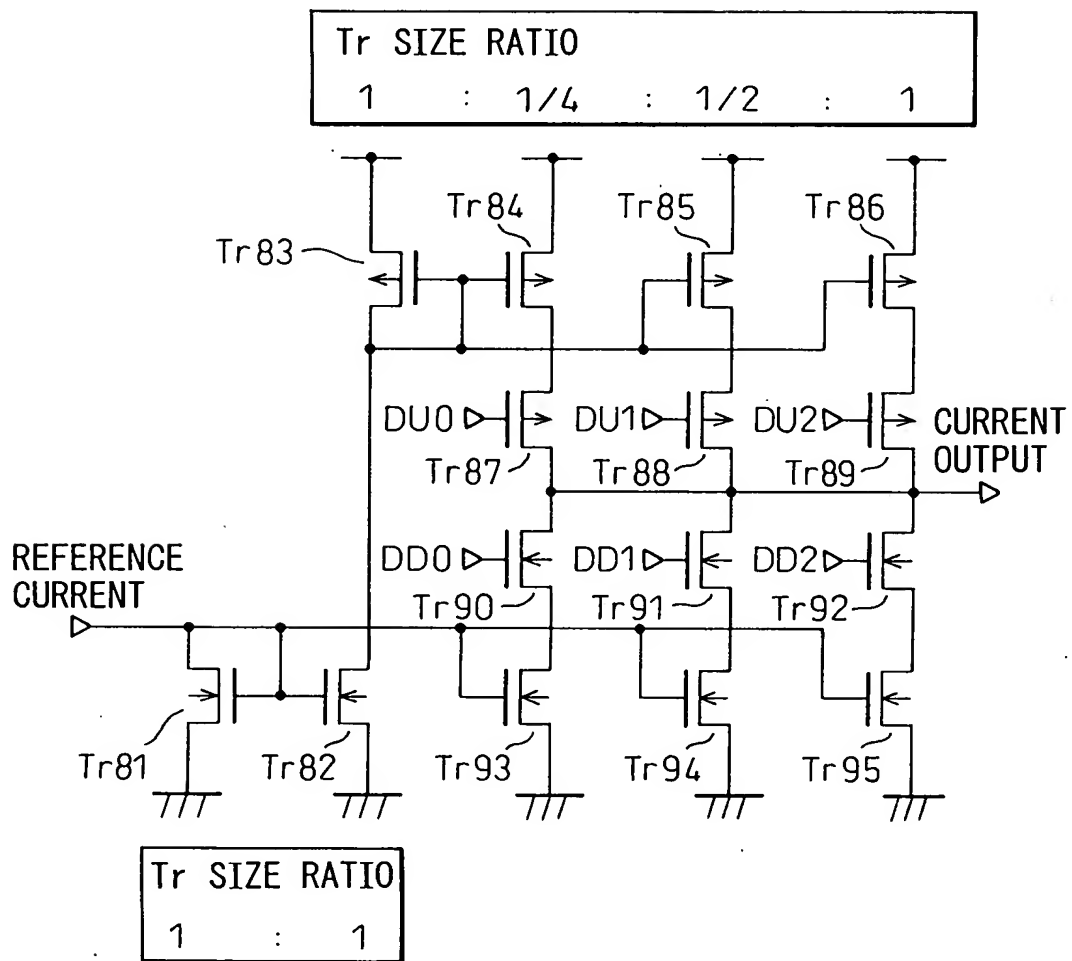


FIG. 49A FIG. 49B FIG. 49C

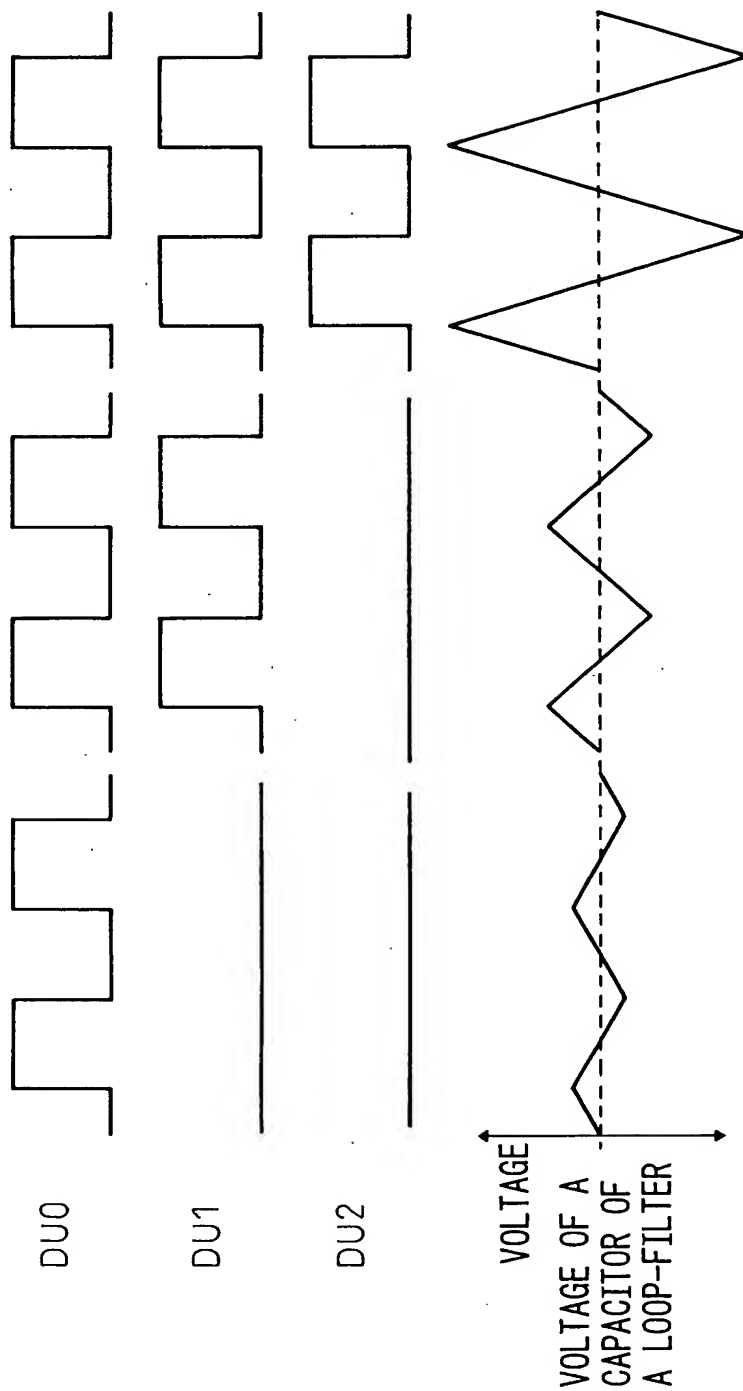


FIG.50

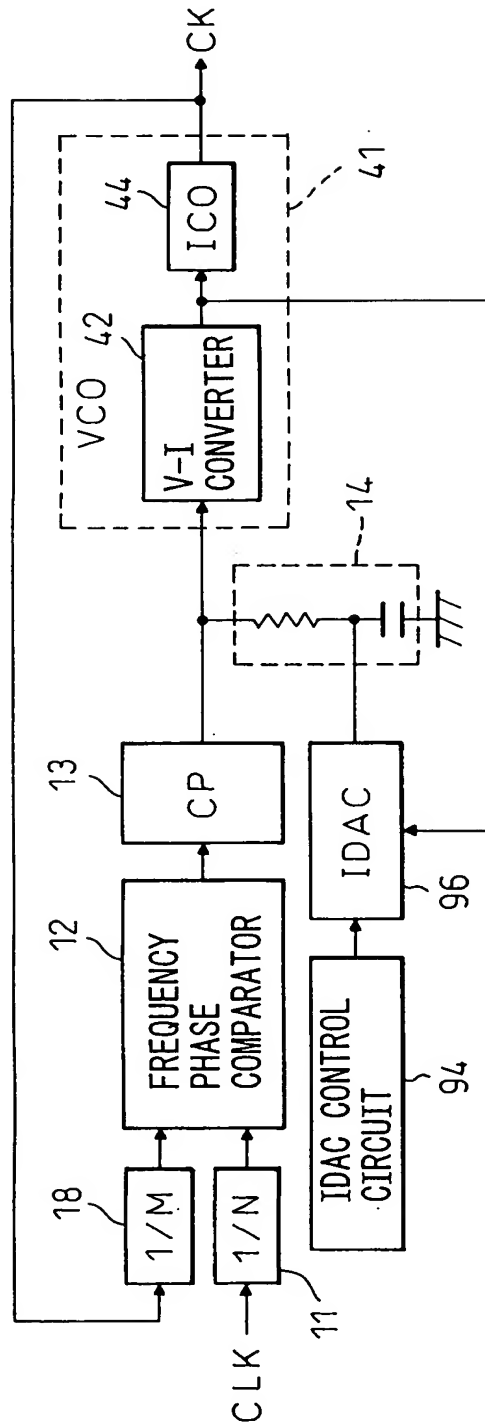


FIG. 51

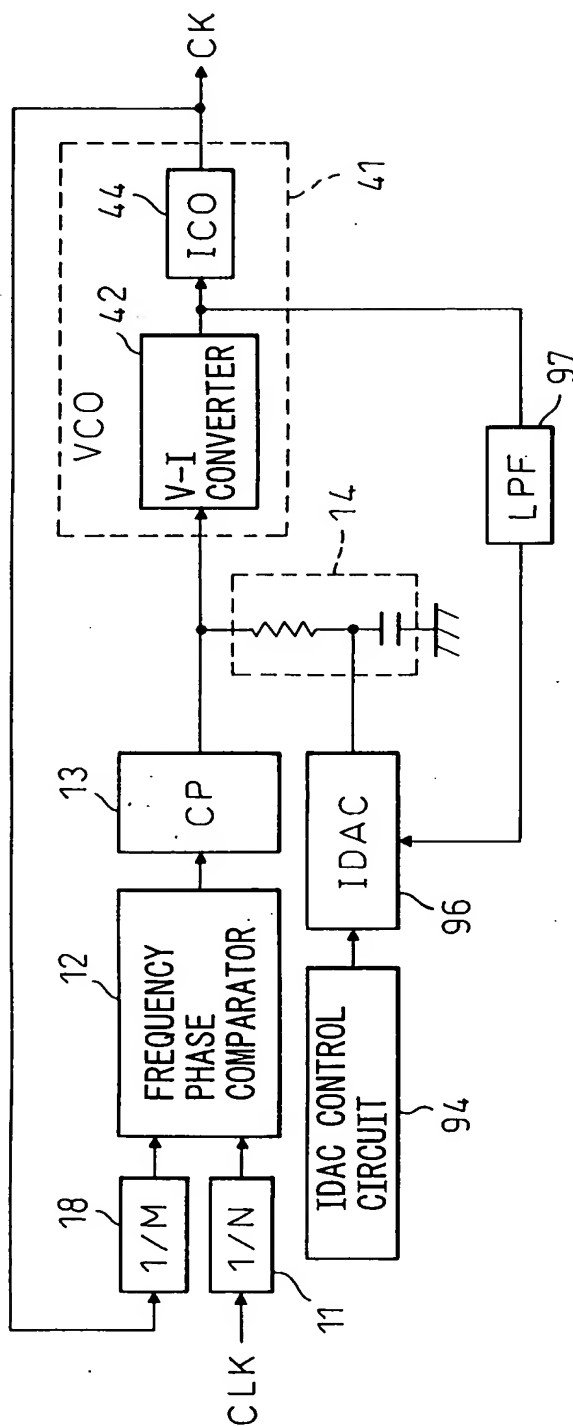


FIG. 52

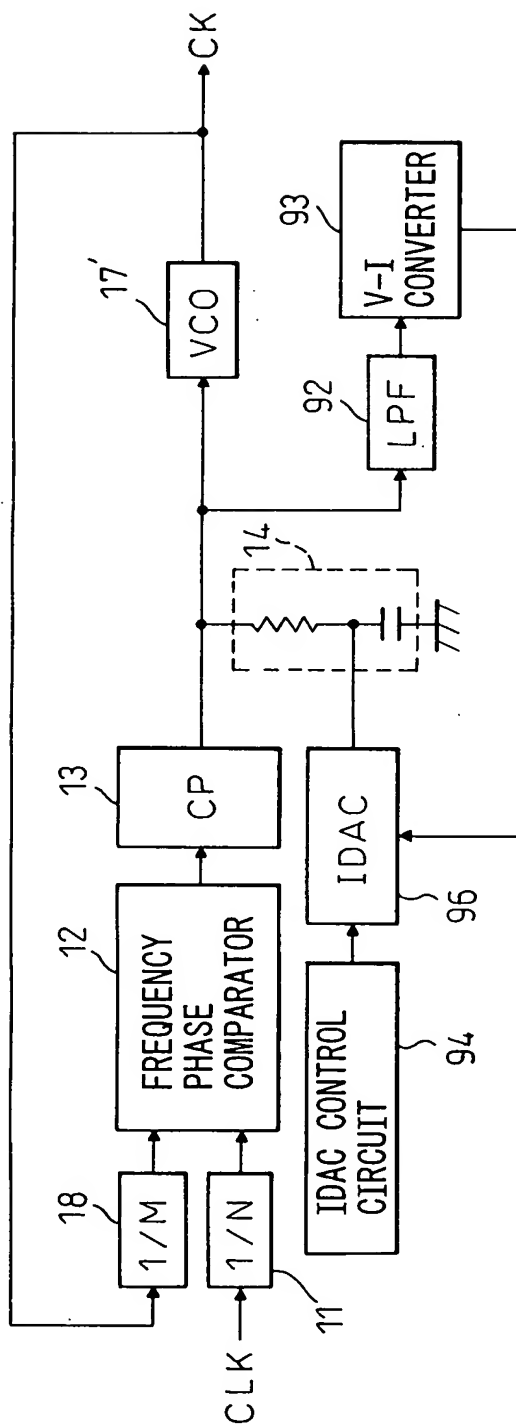


FIG. 53

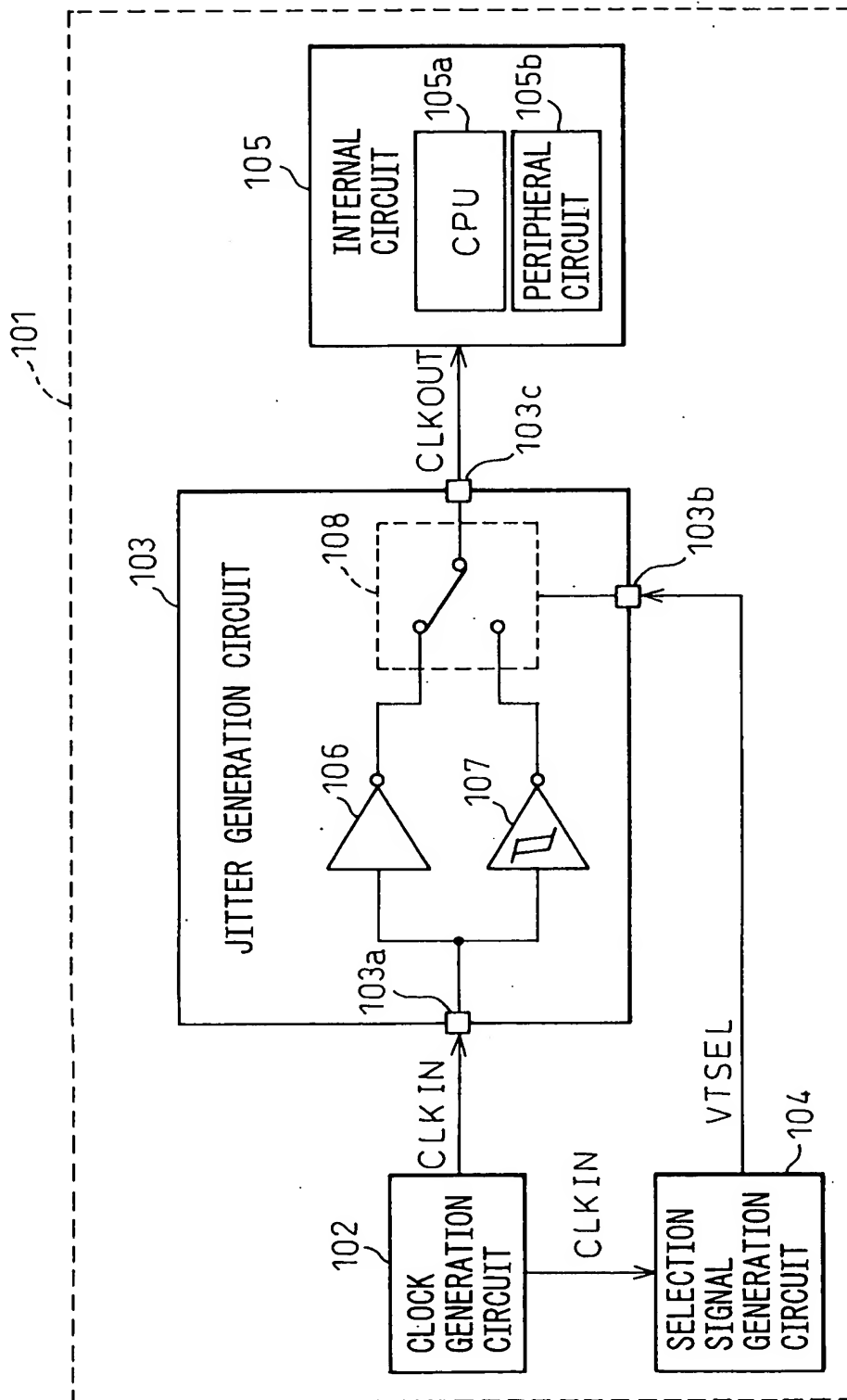


FIG. 54

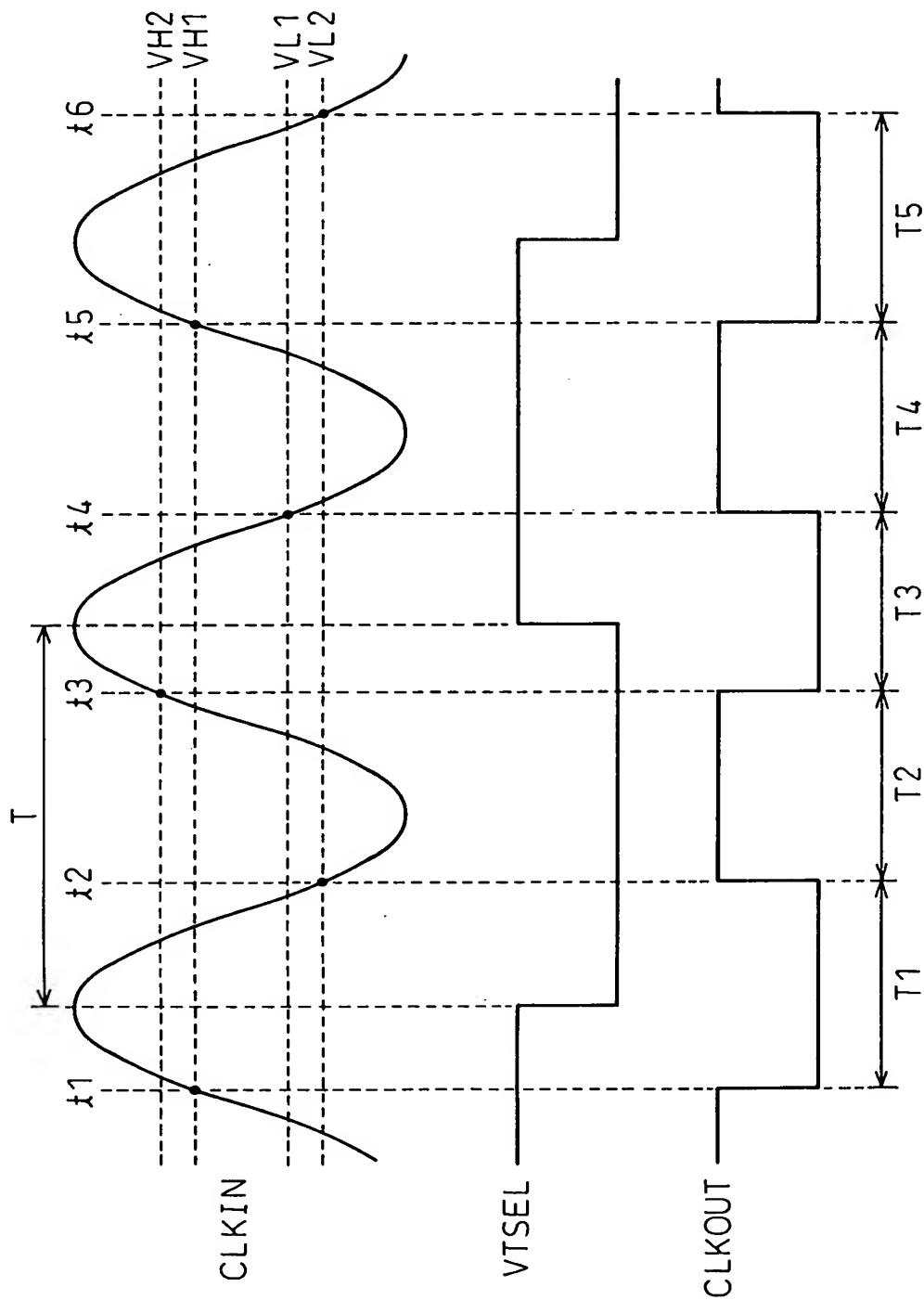


FIG. 55

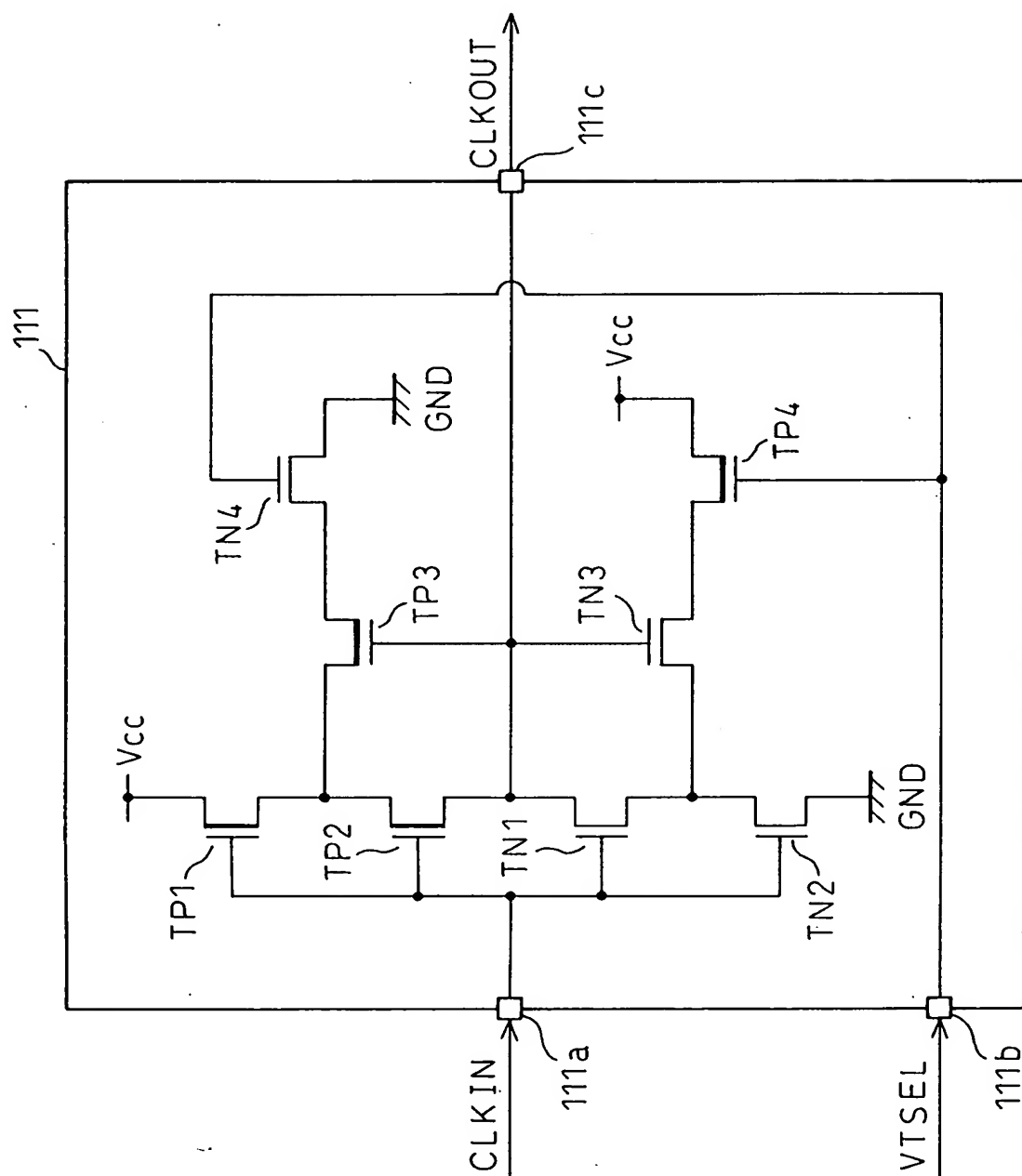
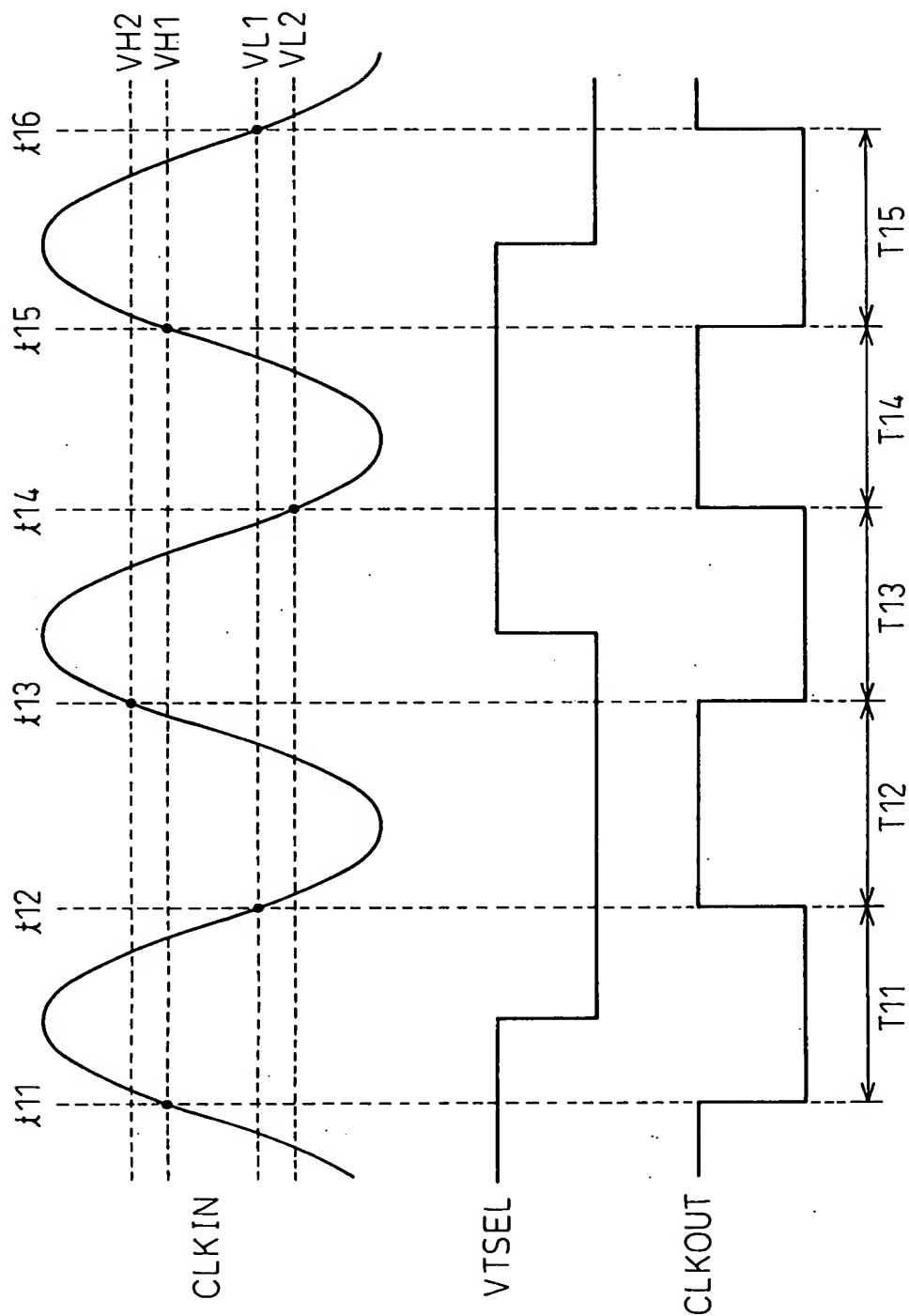


FIG. 56



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FIG. 57

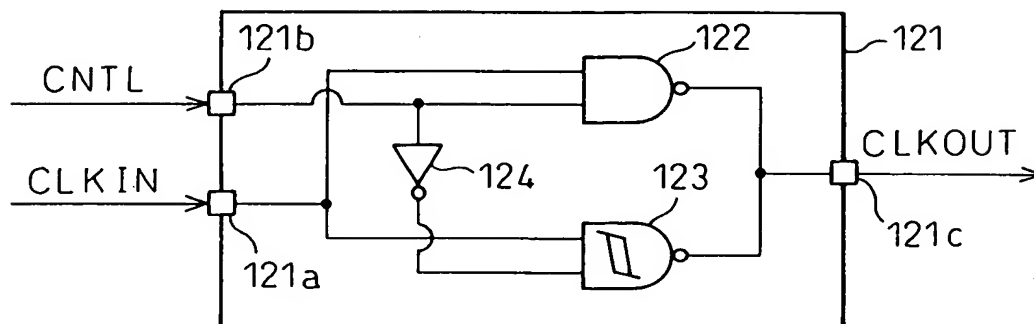


FIG. 58

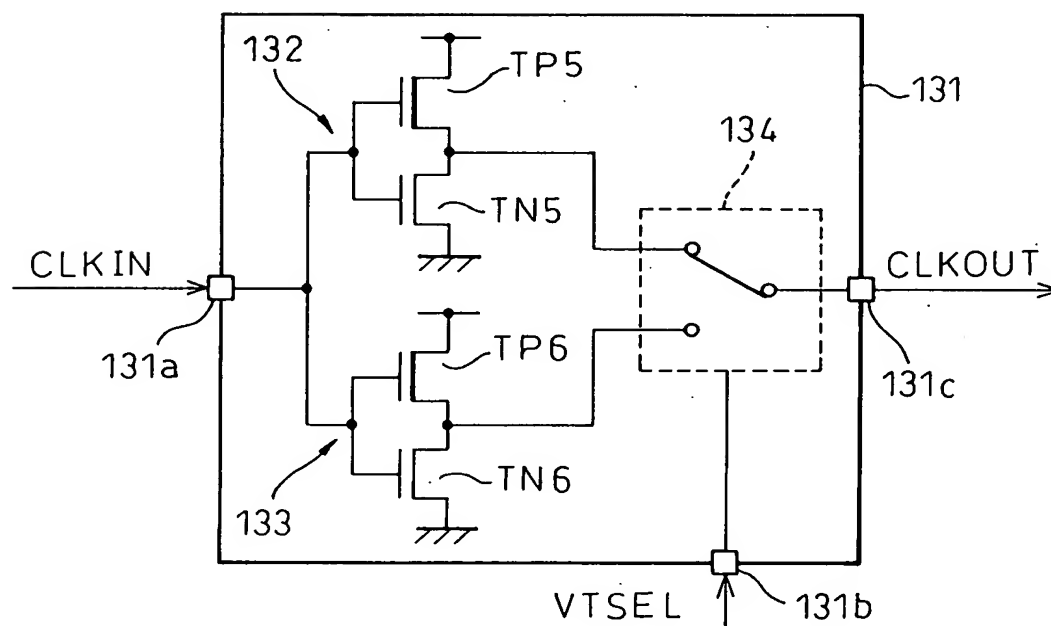


FIG. 59

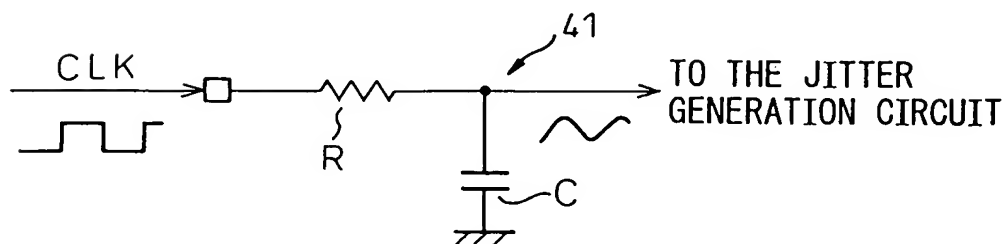


FIG. 60

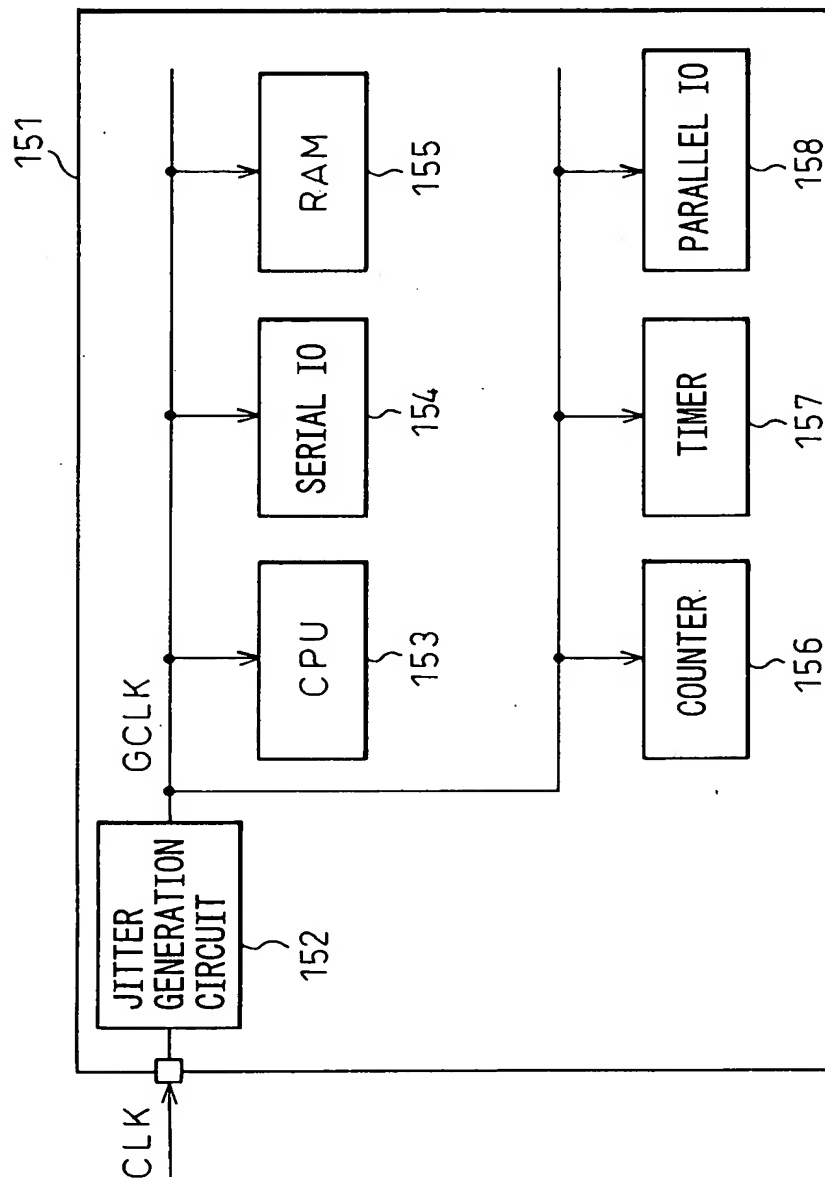


FIG. 61

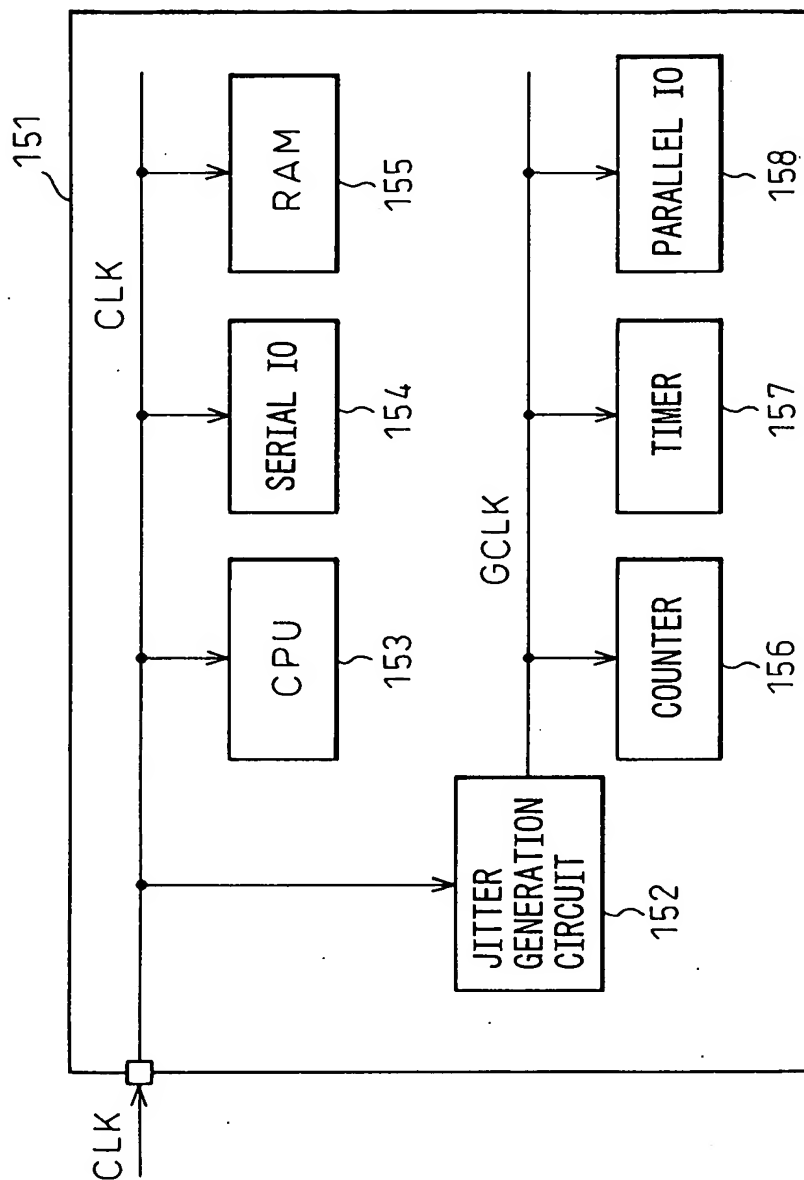


FIG. 62

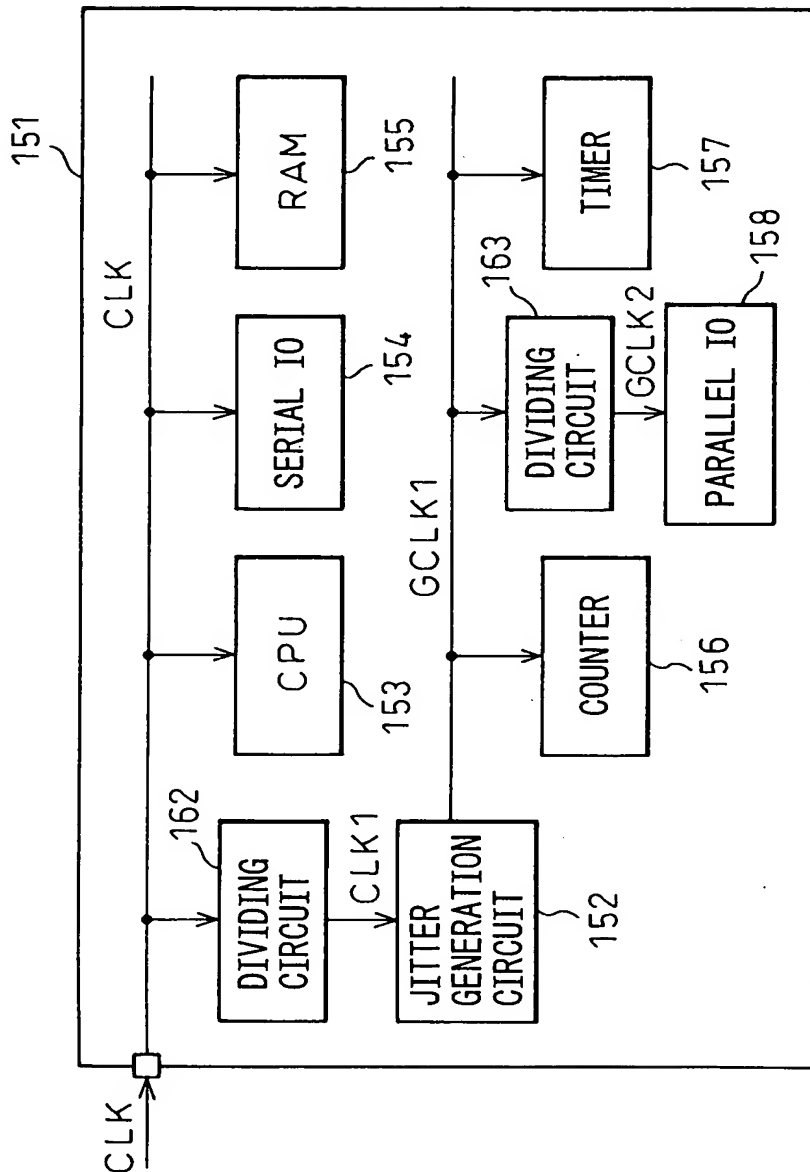


FIG. 63

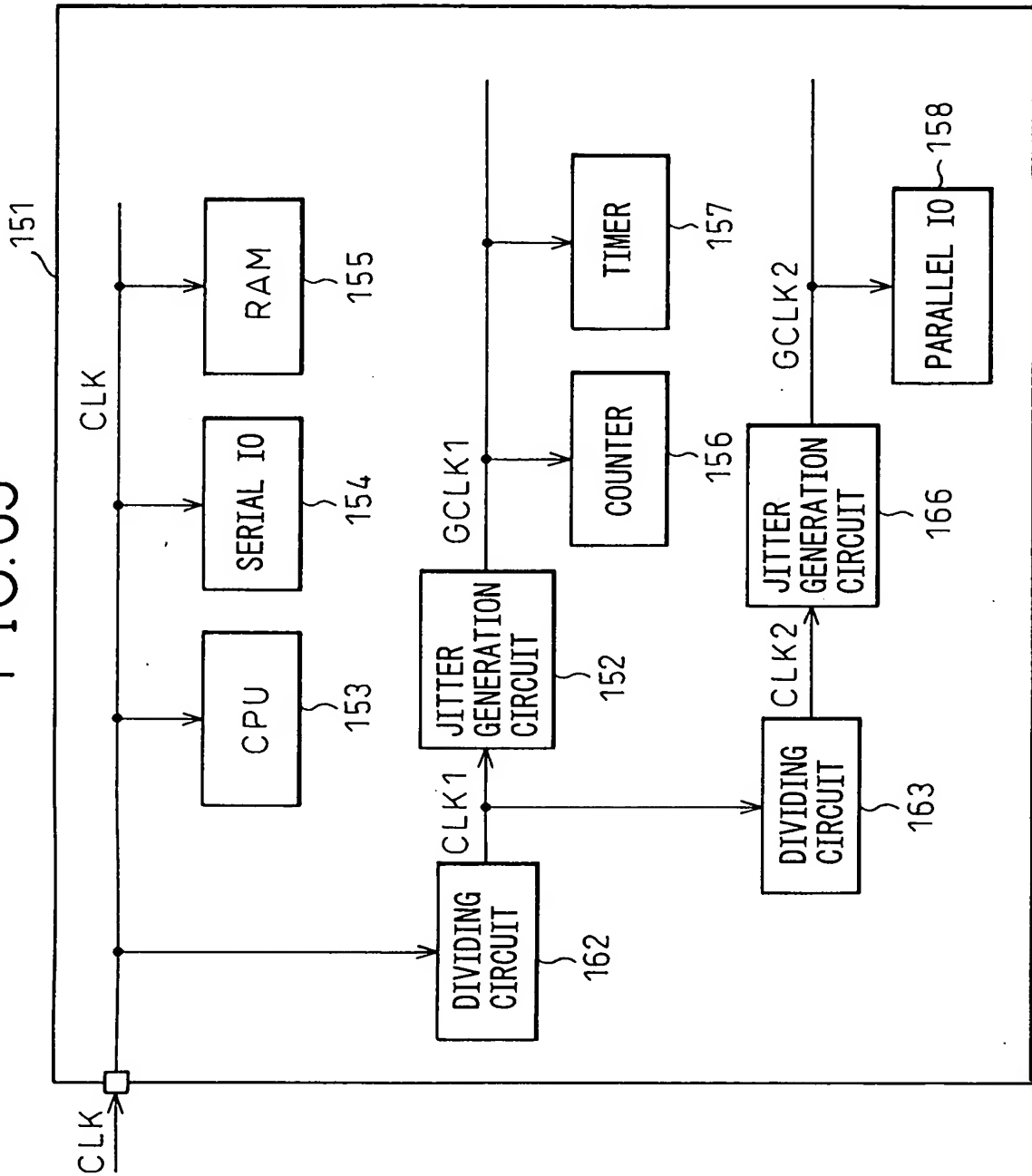


FIG. 64

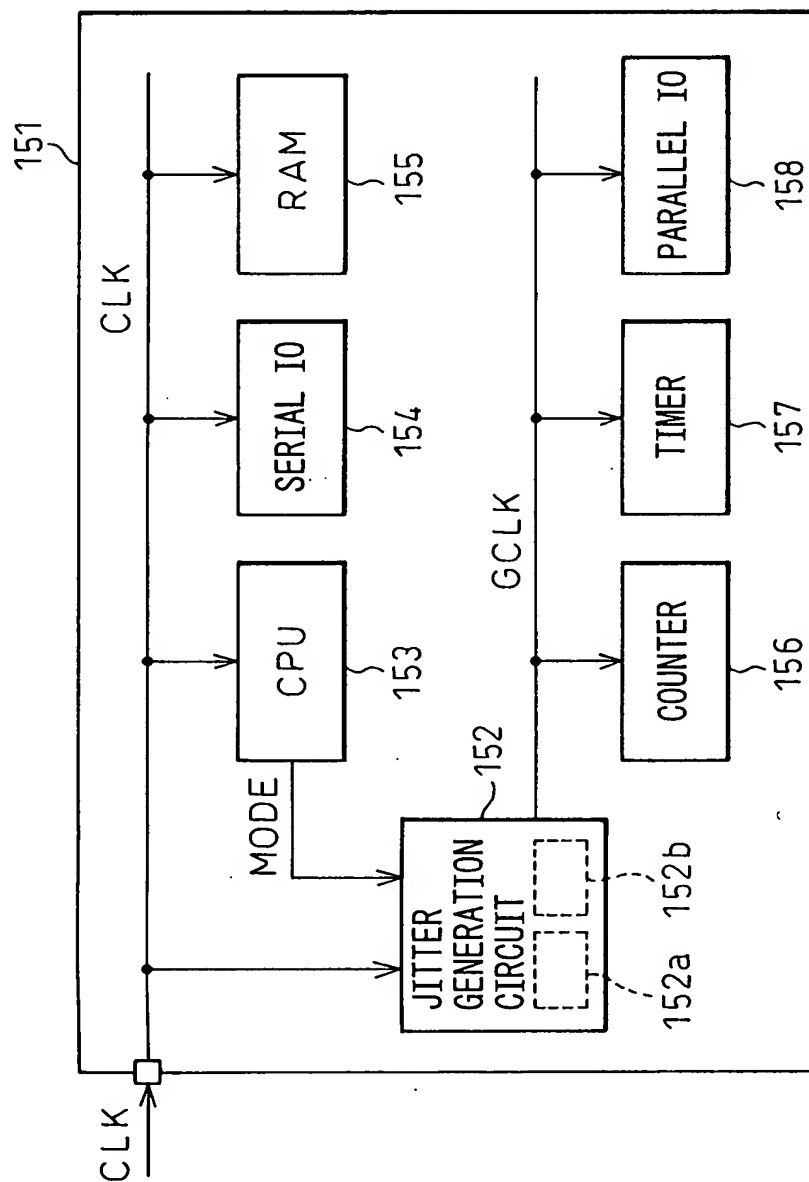


FIG. 65

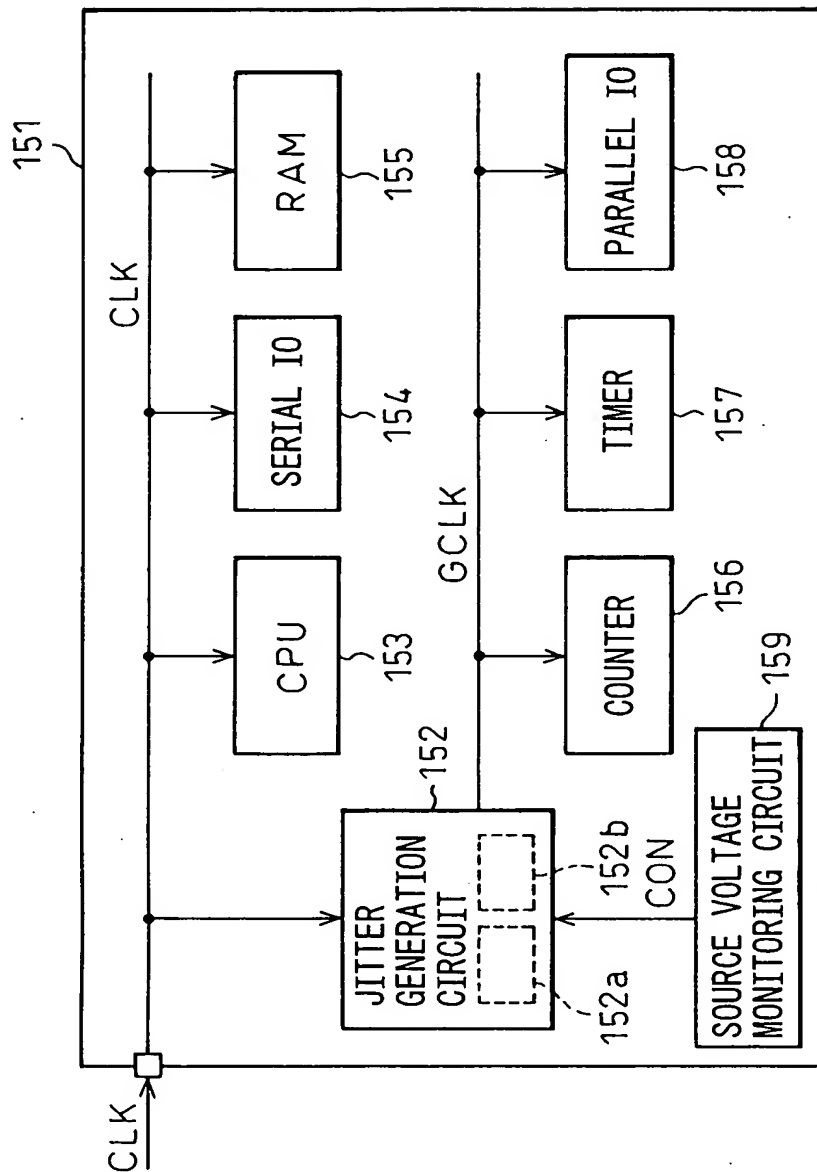


FIG. 66

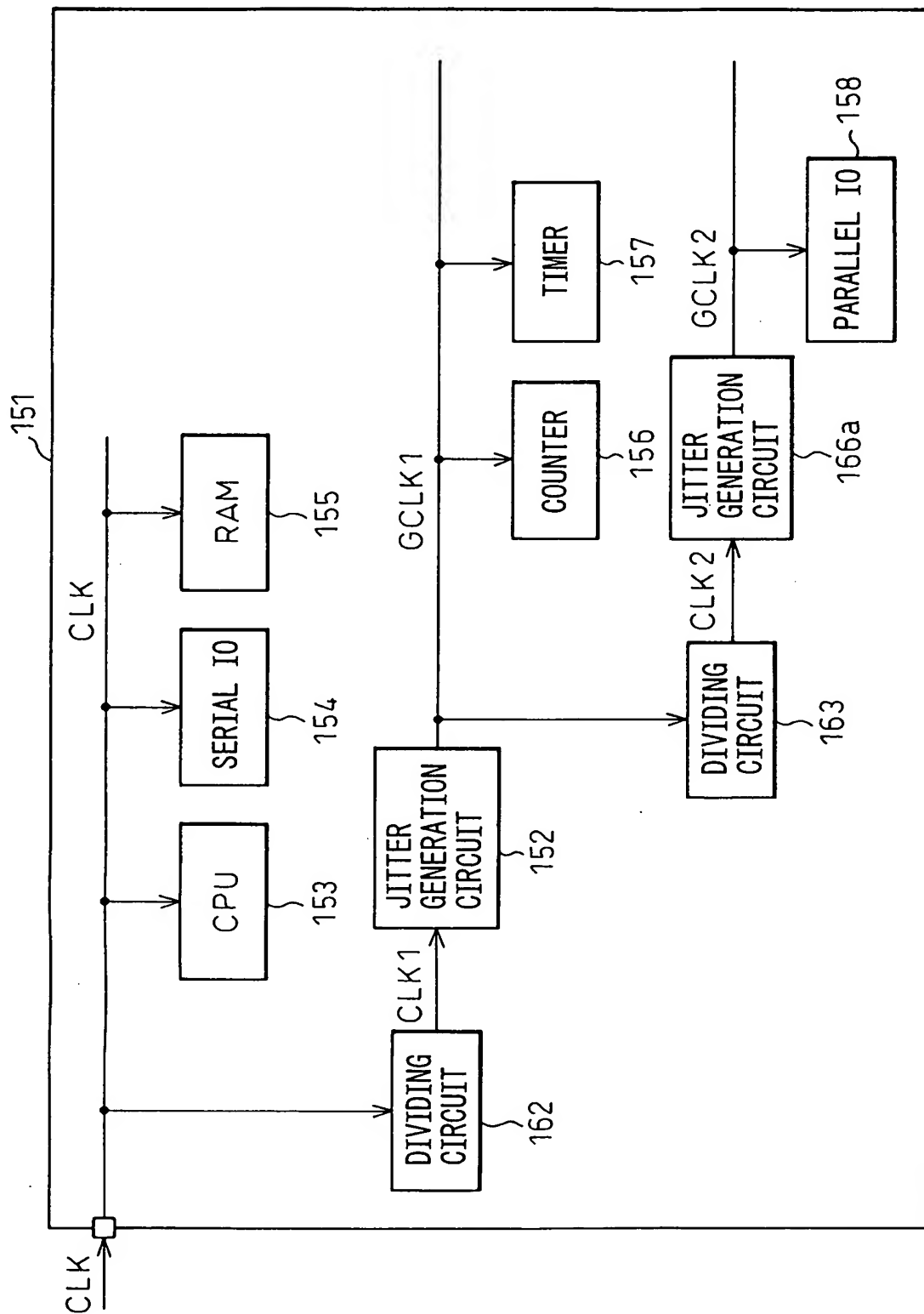


FIG. 67

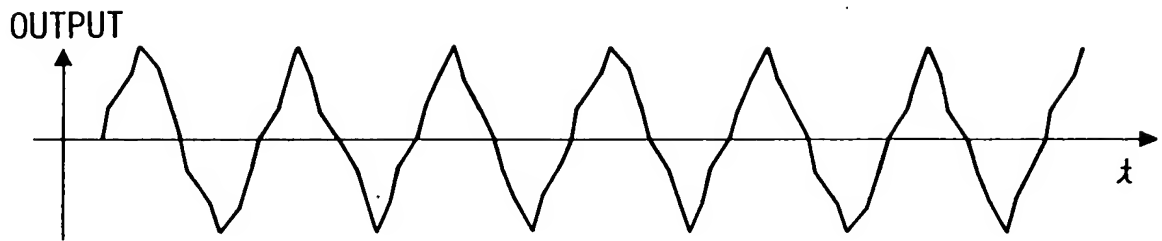


FIG. 68

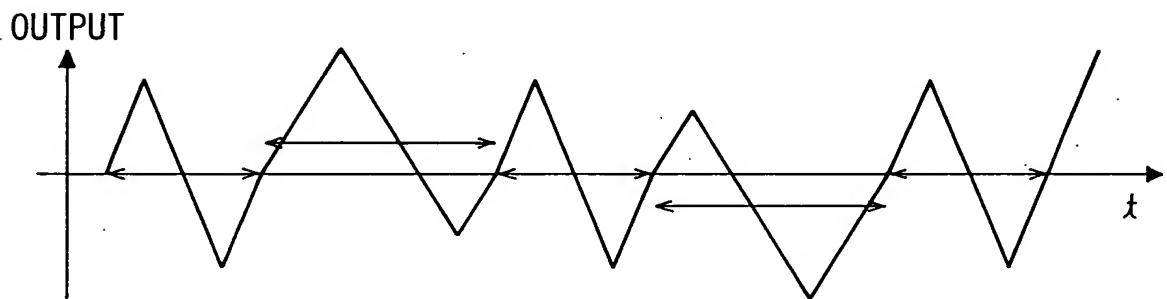


FIG. 69

